FCT LOGIC PRODUCTS

CYPRESS

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FCT Logic Data Book

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General Product Information

CYPRESS SEMICONDUCTOR BACKGROUND

Cypress Semiconductor was founded in April 1983 with the stated goal of serving the high-performance semiconductor market. This market is served by producing the highest-performance integrated circuits using state-of-the-art processes and circuit design. Cypress is a complete semiconductor manufacturer, performing its own process development, circuit design, wafer fabrication, assembly, and test. The company went public in May 1986 and was listed on the New York Stock Exchange in October 1988.

The initial semiconductor process, a CMOS process employing 1.2-micron geometries, was introduced in March 1984. This process is used in the manufacturing of Static RAMs and Logic circuits. In the third quarter of 1984, a 1.2-micron CMOS EPROM process was introduced for the production of programmable products. At the time of introduction, these processes were the most advanced production processes in the industry. Following the 1.2-micron processes, a 0.8-micron CMOS SRAM process was implemented in the first quarter of 1986, and a 0.8-micron EPROM process in the third quarter of 1987.

In keeping with the strategy of serving the high-performance markets with state-of-the-art integrated circuits, Cypress introduced two new processes in 1989. These were a bipolar submicron process, targeted for ECL circuits, and a BiCMOS process to be used for most types of TTL and ECL circuits.

The circuit design technology used by Cypress is also state of the art. This design technology, along with advanced process technology, allows Cypress to introduce the fastest, highest-performance circuits in the industry. Cypress's products fall into six families: high-speed Static RAMs, PROMS, Programmable Logic Devices, Logic, ECL SRAMs and PLDs, and module products. Members of the CMOS Static RAM family include devices in densities of 64 bits to 256K, and performance from 7 ns to 35 ns. The various organizations-x1, x4, x8, and x9-provide optimal solutions for applications such as large mainframes, high-speed controllers and servers, communications, and graphics display. Cypress's BiCMOS family of 64K and 256K SRAMs in x4 and x8 configurations offers speeds as fast as 6 ns. Cypress's cache RAMs include a 4K x 18 cache tag RAM at 10-ns match, a 32K x 9 cache RAM with a 14-ns access time, and an 64K x 18 cache RAM with a 10-ns access time.

Cypress's programmable products consist of high-speed CMOS PROMs employing an EPROM programming element and Programmable Logic Devices (PLDs) based on CMOS EPROM, CMOS FLASH, and BiCMOS Fuse technology. Like the high-speed Static RAM family, these products are the natural choice to replace older devices because they provide superior performance at one half of the power consumption. PROM densities range from 4 kilobits to 512K in byte-wide and x 16 organizations. PLD products range from 20 pins to 84 pins with performance as fast as 5-ns propagation delay and 156-MHz operational frequency. To provide immediate support for new programmable products, Cypress offers our QuickPro II™ programmer (CY3300). QuickPro II is capable of programming all of Cypress's PLDs and PROMs. It uses an IBM PC's® CPU to implement the silicon programming algorithms and interfaces to the PC via the parallel port. The use of an IBM PC as a host allows updating of the programming software using either floppy disk or modem, thereby providing instantaneous support of all new devices. Cypress also offers *Warp2*™ (CY3120), a powerful design entry synthesis and simulation tool for PLDs and state machine PROMs. *Warp2* uses the IEEE-standard (1076) VHDL design language, which is rapidly emerging as the standard language of choice for behavioral design description. Use of the VHDL language allows users the freedom to also use tools from other vendors for design simulation and synthesis. Cypress is the only programmable logic vendor offering VHDL-based design tools.

Logic products include circuits such as 4-bit and 16-bit slices, 16 x 16 multipliers and 16-bit microprogrammable ALUs, a family of 1K/2K x 8 and 4K/8K x 8 dual-port SRAMs, as well as a family of FIFOs that range from 64 x 4 to 32K x 9. Cypress also offers application-specific FIFOs such as the 2K x 9 bidirectional FIFO and the 512/2K x 9 clocked FIFO. FIFOs provide the interface between digital information paths of widely varying speeds. This allows the information source to operate at its own intrinsic speed, while the results may be processed or distributed at a speed commensurate with need.

Cypress's Datacom group has developed a family of 300-MHz point-to-point transmitter/receivers. HOTLink™ is compliant with the IBM ESCON™ and Fibre Channel computer network standards, and will also have applications in military, graphics, and instrumentation systems. The Datacom group is also responsible for the Programmable Skew Clock Buffer, which allows designers to compensate for trace delays and load capacitance in high performance systems.

In late 1993 Cypress acquired the FCT-T and FCT2-T logic product families. They consist of high-performance, low power, CMOS integrated circuits that either meet or exceed the speed and drive capability of their bipolar functional equivalents. Both logic families are TTL compatible. which means that they conform to the industry-standard TTL voltage levels and threshold point, and

operate from a five Volt Vcc power source. All inputs are designed to have 200 mV of hysteresis. The benefit to the user is increased static and dynamic noise immunity, as well as less sensitivity to noise superimposed on slowly rising or falling inputs.

As a result of the acquisition of VTC's manufacturing facility in Minnesota, Cypress has created a VME Bus Interface Products group. Cypress will continue to manufacture VTC's VIC and VAC VME devices on the 0.8-micron CMOS process.

Until 1988, all Cypress products were TTL I/O-compatible. In 1989, Cypress introduced ECL products having access times (propagation delays) of less than 3.5 ns in either of the popular I/O configurations, 100K or 10K/10KH. ECL RAMs include 256 x 4, 1K x 4, and 4K x 4 families with balanced read/write cycles. The RAMs are offered in low-power versions, reducing operating power by 30 percent while achieving 5-ns access times (RAM).

The module family consists of both standard and custom modules incorporating circuits from the other six product families. This capability provides a fast, low-risk solution for designs requiring the ultimate in system performance and density. SRAM and FIFO module configurations are available depending on height and board real estate constraints. Modules include Single-In-Line, Dual-In-Line, Dual Single-In-line, Vertical Dual-In-Line, Quad-In-Line, and (Staggered) Zig-Zag-In-Line packages.

Situated in California's Silicon Valley (San Jose), Round Rock (Austin), Texas, and Bloomington, Minnesota, Cypress houses R&D, design, wafer fabrication, and administration. The facilities are designed to the most demanding technical and environmental specifications in the industry. At the Texas and Minnesota facilities, the entire wafer fabrication area is specified to be a Class 1 environment. This means that the ambient air has less than 1 particle of greater than 0.2 microns in diameter per cubic foot of air. Other environmental considerations are carefully insured: temperature is controlled to a -0.1 degree Fahrenheit tolerance; filtered air is completely exchanged more than 10 times each minute throughout the fab; and critical equipment is situated on isolated slabs to minimize vibration.

Attention to assembly is equally critical. Cypress manufactures 100 percent of our wafers in the United States, at our front-end fabrication sites in California (San Jose), Minnesota (Bloomington), and Texas (Round Rock). Cypress Texas, our largest fab, and Cypress Minnesota, our newest fab, are both Class 1 facilities.

To improve our global competitiveness, we chose to move most of our back-end assembly, test, and mark operations to a facility in Thailand. Be assured that Cypress's total quality commitment extends to the new site-Cypress Bangkok.The move to Bangkok consummated an intense search by Cypress for a world-class, environmentally sophisticated facility that we could bring on line quickly. The Cypress search team scrutinized fifteen manufacturing facilities in five countries and chose a site managed by Alphatec Electronics Co., Ltd., a privately owned, entrepreneurial company promoted by the Thailand Board of Investment. Cypress Bangkok occupies almost 25,000 square feet-a significant portion of the manufacturing floor space available within the facility. The full facility at Bangkok occupies more than 85,000 square feet on a site that encompasses 25 acres-sufficient room for expansion to a number of buildings in a campus-like setting.

Manufacturing at the site since 1990 with a charter to specialize in IC packaging, the Alphatec facility has almost a century of person-years experience working for U.S. semiconductor suppliers. Thoroughly modern, MIL 883-certified, and with fully developed administrative, logistic, and manufacturing systems in place, the facility has earned an exceptional reputation for hermetic assembly and out-going quality.

Cypress San Jose maintains complete management control of Cypress Bangkok's assembly, test, mark, and ship operations within the facility, thus assuring complete continuity of San Jose's back-end operations and quality.

Cypress has added Tape Automated Bonding (TAB) to it package offering. TAB, a surface-mount packaging technology, provides the densest lead and package footprint available for fully tested die.

As a result of the acquisition of VTC's manufacturing facility in Minnesota, Cypress has created a VME Bus Interface Products group. Cypress will continue to manufacture VTC's VIC and VAC VME devices on the 0.8 micron CMOS process.

The Cypress motto has always been "only the best-the best facilities, the best equipment, the best employees . . . all striving to make the best CMOS and BiCMOS products.

Cypress Process Technology

In the last decade, there has been a tremendous need for high-performance semiconductor products manufactured with a balance of SPEED, RELIABILITY, and POWER. Cypress Semiconductor overcame the classically held perceptions that CMOS was a moderate-performance technology.

Cypress initially introduced a 1.2-micron "N" well technology with double-layer poly and a single-layer metal. The process employed lightly doped extensions of the heavily doped source and drain regions for both "N" and "P" channel transistors for significant improvement in gate delays. Further improvements in performance, through the use of substrate bias techniques, have added the benefit of eliminating the input and output latch-up characteristics associated with older CMOS technologies.

Cypress pushed process development to new limits in the

areas of PROMs (Programmable Read Only Memory) and EPLDs (Eraseable Programmable Logic Devices). Both PROMs and EPLDs have existed since the early 1970s in a bipolar process that employed various fuse technologies and was the only viable high-speed nonvolatile process available. Cypress PROMs and EPLDs use EPROM technology, which has been in use in MOS (Metal Oxide Silicon) since the early 1970s. EPROM technology has traditionally emphasized density while forsaking performance. Through improved technology, Cypress produced the first high-performance CMOS PROMs and EPLDs, replacing their bipolar counterparts.

To maintain our leadership position in CMOS technology, Cypress introduced a sub-micron technology in 1987. This 0.8 micron breakthrough made Cypress's CMOS one of the most advanced production processes in the world. The drive to maintain leadership in process technology has not stopped with the 0.8-micron devices. Cypress introduced a 0.65-micron process in 1991. A 0.5-micron process is currently in the works.

Although not a requirement in the high-performance arena, CMOS technology substantially reduces the power consumption for any device. This improves reliability by allowing the device to operate at a lower die temperature. Now higher levels of integration are possible without trading performance for power. For instance, devices may now be delivered in plastic packages without any impact on reliability.

While addressing the performance issues of CMOS technology, Cypress has not ignored the quality and reliability aspects of technology development. Rather, the traditional failure mechanisms of electrostatic discharge (ESD) and latch-up have been addressed and solved through process and design technology innovation.

ESD-induced failure has been a generic problem for many high-performance MOS and bipolar products. Although in its earliest years, MOS technology experienced oxide reliability failures, this problem has largely been eliminated through improved oxide growth techniques and a better understanding of the ESD problem. The effort to adequately protect against ESD failures is perturbed by circuit delays associated with ESD protection circuits. Focusing on these constraints, Cypress has developed ESD protection circuitry specific to 1.2-, 0.8-, 0.65-, and 0.5-micron CMOS process technology. Cypress products are designed to withstand voltage and energy levels in excess of 2001 volts and 0.4 milli-joules.

Latch-up, a traditional problem with CMOS technologies, has been eliminated through the use of substrate bias generation techniques, the elimination of the "P" MOS pull-ups in the output drivers, the use of guardring structures and care in the physical layout of the products.

Cypress has also developed additional process innovations and enhancements: multilayer metal interconnections, advanced metal deposition techniques, silicides, exclusive use of plasma for etching, and 100-percent stepper technology with the world's most advanced equipment.

Cypress technologies have been carefully designed, creating products that are "only the best" in high-speed, excellent reliability, and low power.

PARAMETER MEASUREMENT INFORMATION
(FCT-T AND FCT2-T LOGIC-- ULTRA HIGH SPEED, LOW-NOISE CMOS LOGIC)

FEATURES

- **Function, Pinout, Speed and Drive Compatible with F Logic**
- **Meets Requirements of FCT Logic JEDEC Standard No. 18A**
- **Edge-rate control circuitry for significantly improved noise characteristics (FCT-T/FCT2-T)**
- **Power-off disable feature (FCT-T/FCT2-T)**
- **Matched Rise and Fall times**
- **CMOS for Low Power Consumption - Typically 1/3 of the Fastest Advanced Schottky TTL Logic**
- **Inputs and Outputs Interface Directly with TTL, NMOS and CMOS Devices**
- **Typically 64 mA Sink and 15 mA Source Drive Capability (FCT-T)**
- **3-State Outputs on Most Devices**
- **Operational over the full Commercial and Military Temperature Ranges**
- **Products Available to Latest Revision of MIL-STD-883 Class B Compliance**

DESCRIPTION

Overview of FCT-T and FCT2-T Logic Families.

FCT-T and FCT2-T are logic families consisting of high-performance, low power, CMOS integrated circuits that either meet or exceed the speed and drive capability of their bipolar functional equivalents. These families represent a "technology crossover point" that occured when the performance achieved using CMOS technology matched that of bipolar technology, and at typically one-third the power.

Both logic families are TTL compatible, which means that they conform to the industry-standard TTL voltage levels and threshold point, and operate from a five Volt V_{cc} power source. The TTL threshold point is 1.5 Volts. All inputs are designed to have 200 mV of hysterisis, which means that the low to high threshold point is 1.6 V and the high to low threshold point is 1.4 V. The benefit to the user is increased static and dynamic noise immunity, as well as less sensitivity to noise superimposed on slowly rising or falling inputs.

The FCT-T logic family features output buffers that use n-channel pullup transistors and controlled rise and fall time edge rates. Typical unloaded output signal rise and fall times are two nanoseconds. The maximum unloaded output high voltage, V_{OH}, is V_{cc} minus the n-channel threshold, V_T. The transistor drain is connected to V_{cc}, so V_T is approximately one volt worst case and typically 0.5 V. The loaded V_{OH} is typically 3.3 Volts when sourcing 15 mA with a V_{cc} of 4.95 V.

The reduced output voltage swing of FCT-T results in lower crosstalk. The controlled edge rates reduce crosstalk as well as groundbounce.

The FCT2-T logic family is identical to the FCT-T logic family, except that the FCT2-T devices have a 25 Ohm resistor in series with the output. The purpose of the resistor is to provide series damping when driving a transmission line. These products with series damping resistors should be used only when driving lumped (or single) loads, and should not be used for driving multiple or distributed loads. For a description of series damping, see the application note *System Design Considerations When Using Cypress CMOS Circuits* in the *Cypress Applications Handbook.*

CMOS Process Technology

The FCT-T and FCT2-T products are manufactured using the Logic 2.7 process and are fabricated in a Class 1 facility on six inch wafers. The minimum drawn channel length is 0.65 microns and the effective channel length is 0.5 microns. The process uses one layer of polysilicon and two layers of metal. There is no substrate bias generator. In addition to providing high density, the technology assures latch-up protection, single event upset protection, and excellent ESD protection.

Switching Characteristics

The circuit of Figure 1 is used to load each output for specifying and measuring device propagation delays. It is a de facto industry standard and does not represent device behavior in any application.

The switch is open for all measurements except those having to do with the outputs entering or leaving the high impedance state as a result of a control input changing. These conditions are illustrated in Figures 7 and 8. The parameter t_{PZL} is the amount of time it takes an output to go from the high-impedance state to a low state. The parameter t_{PLZ} is the amount of time it takes an output to go from the low state to the high-impedance state; defined as 300 mV above V_{OL}. The parameter t_{PZH} is the amount of time it takes an output to go from the high-impedance state to a high

state. The parameter t_{PHZ} is the amount of time it takes an output to go from a high state to the high-impedance state; defined as 300 mV below V_{OH}.

Figures 2 through 9 illustrate the various propagation delay, setup times, and hold times that are referred to in the Switching Characteristics section of the various FCT2-T and FCT-T data sheets. Note that except for entering the high-impedance state, all measurements are made between the 1.5 Volt amplitude voltage levels.

The input waveform amplitude levels recommended for AC testing of Cypress logic products are illustrated in Figure 10. Input signals should have maximum rise and fall times of 2.5 ns and signal swings of zero to three volts. Input signals with rise and fall times of one nanosecond should be used for testing minimum pulse width or maximum frequency.

When performing AC tests, care must be taken to insure that the input signals do not return to the transition region due to signal overshoot or undershoot. It is recommended that the load capacitor be a leadless "chipcap." If this is not possible, keep the leads as short as possible in order to avoid signal overshoot and undershoot due to lead inductance. The same reasoning applies to the load resistors and power supply decoupling and filtering capacitors. Solid grounding is required and a ground plane is recommended.

Power Specifications

Cypress logic devices do not use a substrate bias generator. As a result, the quiescent or standby current is typically a few microamperes when the voltage at the inputs are either less than 0.2 V or greater than V_{cc}-0.2 V. On the data sheet this current is described as "Quiescent Power Supply Current", given the symbol I_{cc}, and specified on a per IC basis. No inputs are switching and all outputs are open, and if possible, disabled.

When the input signal transitions between the logic levels, both the p-channel pullup transistor and the n-channel pulldown transistor in the input TTL to CMOS translator are partially turned on, which creates a low impedance path between V_{cc} and ground. On the data sheet this current is described as "Quiescent Power Supply Current (TTL inputs)" , given the symbol ΔI_{cc}, and specified on a "per input" basis. One input is at V_{IN} = 3.4 V and all other inputs at either V_{cc} or 0 volts, and all outputs are open, and if possible, disabled.

The "Dynamic Power Supply Current", given the symbol I_{CCD}, is not measured directly, but is provided so that the user can calculate total current. It is specified in mA per Megahertz at 50% duty cycle, with one input toggling and one output toggling (enabled) but open (unloaded).

Note that the preceding three currents are specified with the outputs open. The AC, CVf current required to charge and discharge parasitic capacitances (e.g. other inputs being drivin by the outputs), as well as any DC load currents must be calculated separately.

Total supply current, I_c, is specified on the data sheet for several different conditions. The inputs are switched between ground and either TTL (3.4 V) or CMOS (V_{cc} - 0.2 V) levels with rise and fall times of 2.5 ns. Slow rise and fall times can cause the dynamic current to increase, because the input signals are within the transition region for longer times. A characterization curve of normalized ($I_{cc}/\Delta I_{cc}$) currents versus V_{IN} is shown in Figure 14.

Total device current can be estimated by using the following formula to calculate the total current. This equation implies calculating the current associated with each input and adding them up. The same procedure must be followed to calculate the CVf current required to charge and discharge the load capacitances.

Where;

I_{cc} = Quiescent Current

ΔI_{cc} = Power Supply Current for a TTL HIGH input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL inputs HIGH

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)

f_{cp} = Clock frequency for registered devices, otherwise zero

f_n = Input signal frequency

N_n = Number of inputs changing at F_n

ESD (Electrostatic Discharge) Precautions

Large electrical fields can damage the thin gate oxides of MOS transistors. Special input protection circuits are used at every input pin of all Cypress products to provide protection against ESD. This circuitry has been designed to withstand repeated applications of high voltages without failure or performance degradation. This is accomplished by preventing the high voltage (ESD) from reaching the thin gate oxides of the internal transistors. For a description of the ESD protection circuit and an explanation of its operation, please see the application note titled *Input/ Output Characteristics of Cypress Circuits* in the Cypress *Applications Handbook.*

Precautions should be taken by persons handling CMOS devices. It is recommended that individuals wear a grounded wrist strap or ankle strap when handling Cypress FCT-T or FCT2-T devices.

RECOMMENDED OPERATING CONDITIONS[3]

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1901 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1901 Tbl 04

Notes:

3. Unless otherwise restricted or extended by detail specifications.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
V_{IN}	Input Voltage	–0.5 to +7.0V	V

1901 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
I_{IN}	Input Current	–30 to +5.0	mA
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1901 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

FIGURES

Fig. 1 Test Load

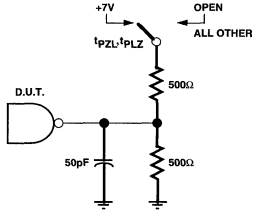


Fig. 2 Waveform for Inverting Functions

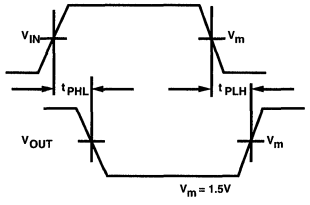


Fig. 3 Waveform for Non-Inverting Functions

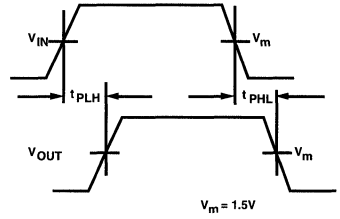


Fig. 4 Setup and Hold Times, Rising-Edge Clock

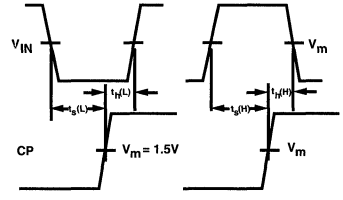


Fig. 5 Proportion Delays from Rsing-Edge Clock or Enable

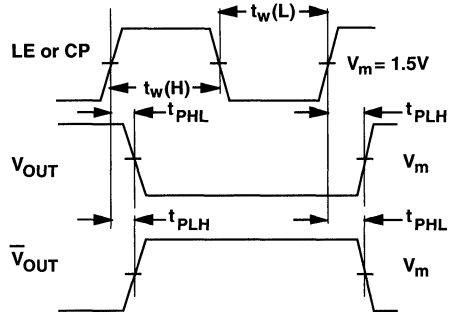


Fig. 6 Asynchronous Reset, Active Rising-Edge Clock or Active LOW Enable

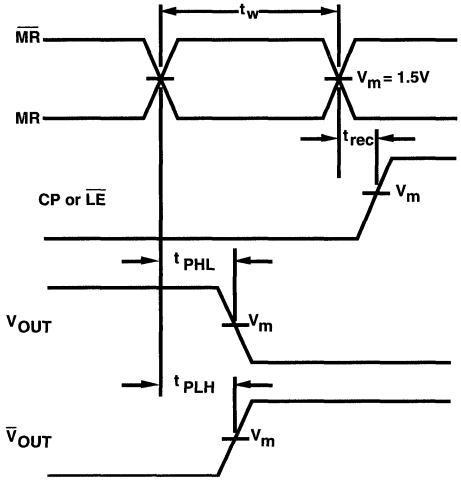


Fig. 7 3-State Output LOW Enable and Disable Times

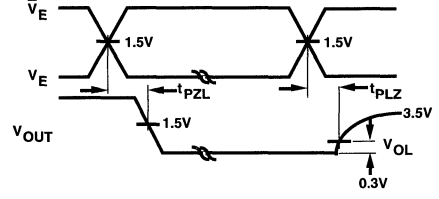


Fig. 8 3-State Output HIGH Enable and Disable Times

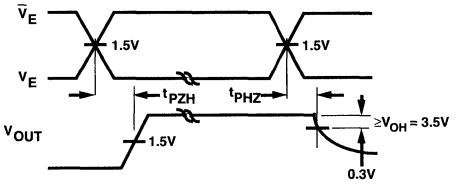


Fig. 9 Setup and Hold Times to Active HIGH Enable or Parallel Load

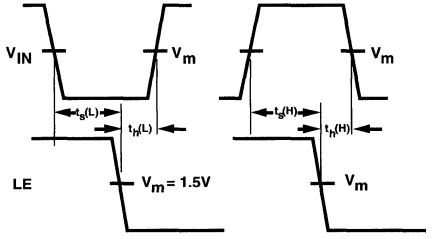
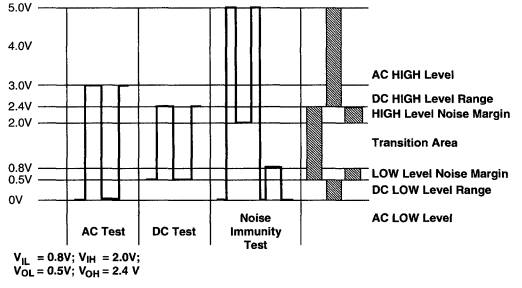


Fig. 10 Input Signal Levels



TYPICAL AC AND DC CHARACTERISTICS

Fig. 11 output source current vs. output voltage

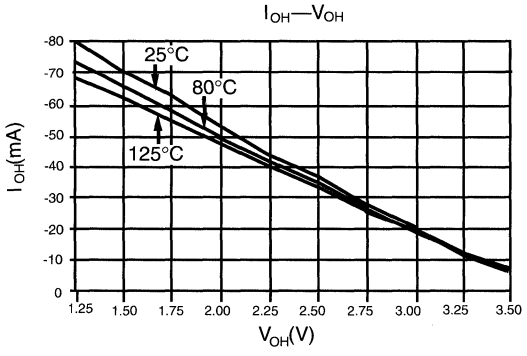


Fig. 14

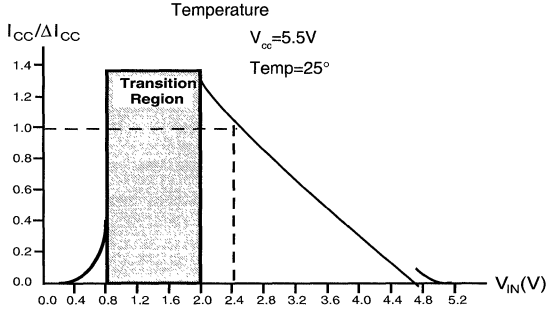


Fig. 12 Normalized Propagation delay vs V_{cc}

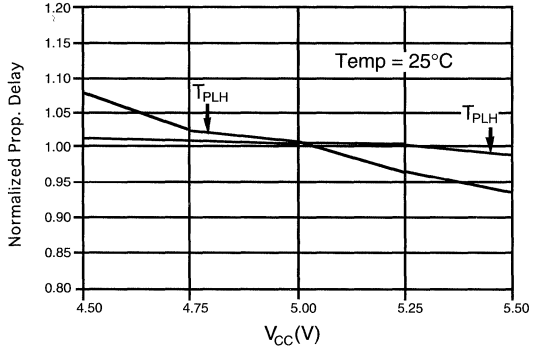


Fig. 15 Normalized Propagation delay vs. temperature

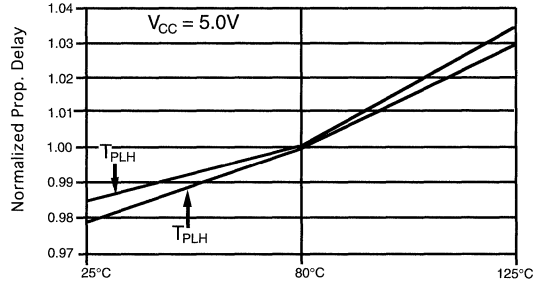


Fig. 13 Normalized Propagation delay vs output loading

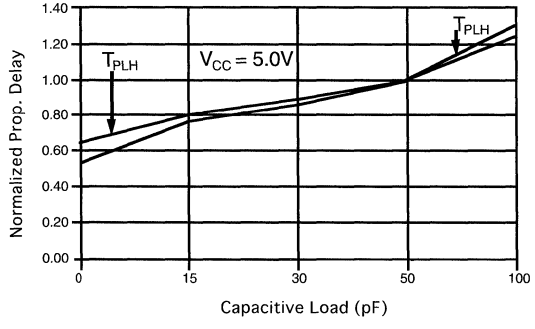
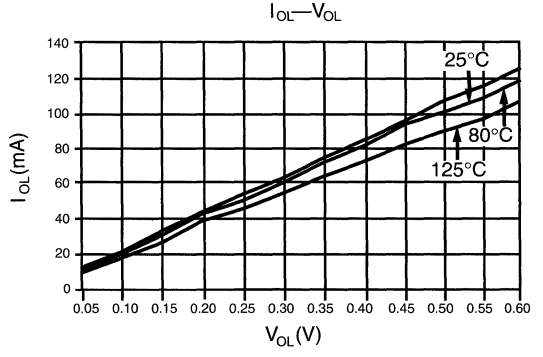
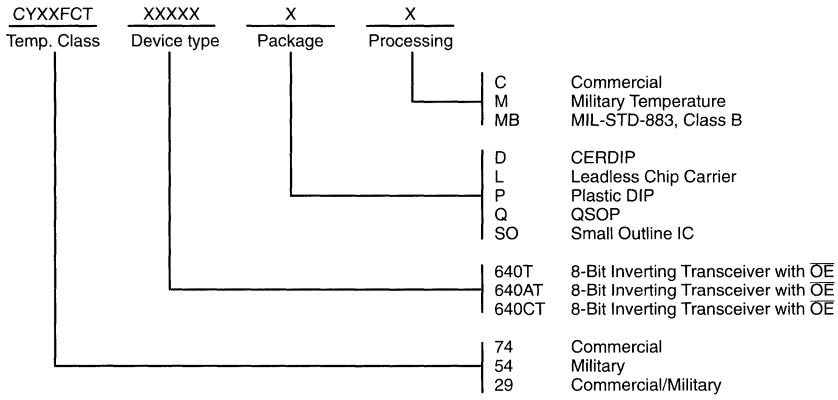


Fig. 16 Output sink current vs. output voltage

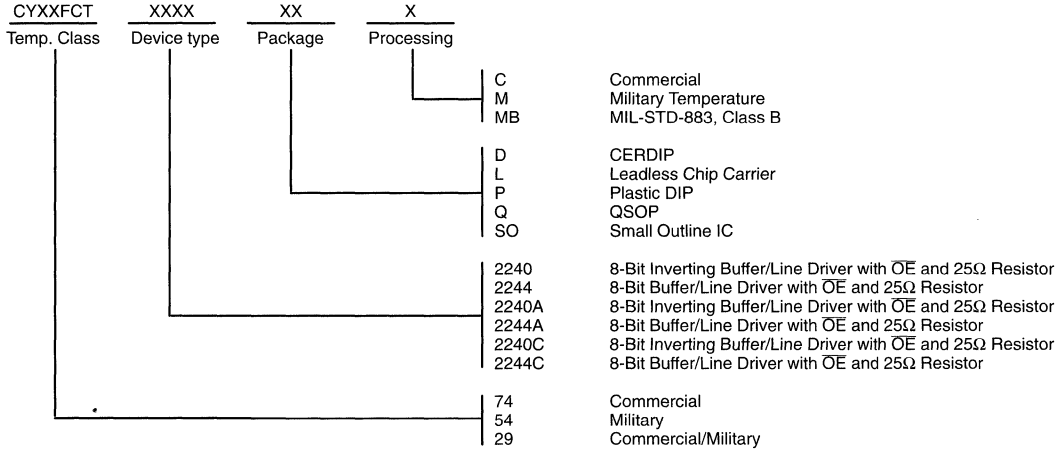


Logic Ordering Information

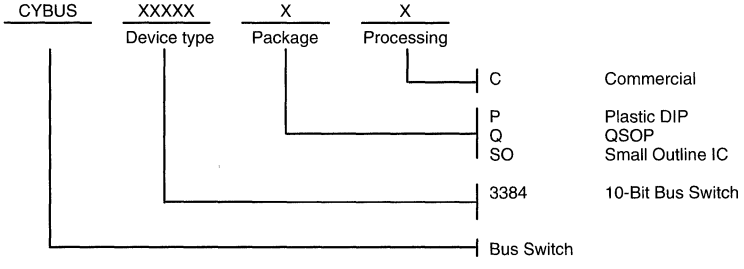
FCT–T



FCT–2



3384



FCT–T Logic Products (V_{CC}=5 Volts)

			Propagation Delays (ns)							
			C		B		A		Standard	
Part Number	Organization	Pins	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
CY29FCT52T	8-Bit Registered Transceiver	24	6.3	7.3	7.5	8.0	10.0	11.0		
CY29FCT520T	Multilevel Pipeline Register	24	6.0	7.0	7.5	8.0	14.0	16.0		
CY29FCT818T	Diagnostic Scan Register	24	6.0	7.6	7.5	9.0	9.0	12.0	13.0	18.0
CY54/74FCT138T	1-of-8 Decoder	16	5.0	6.0			5.8	7.8	9.0	12.0
CY54/74FCT157T	Quad 2-input Multiplexers	16	4.3	5.0			5.0	5.8	6.0	7.0
CY54/74FCT158T	Quad 2-input Inverting Multiplexers	16	4.3	5.5			5.5	6.3	6.5	7.5
CY54/74FCT163T	4-Bit Binary Counter with Synchronous Reset	16	5.8	6.1			7.2	7.5	11.0	11.5
CY54/74FCT191T	4-Bit Up/Down Binary Counter	16	6.2	8.4			7.8	10.5	12.0	16.0
CY54/74FCT240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$	20	4.3	4.7			4.8	5.1	8.0	9.0
CY54/74FCT244T	8-Bit Buffer/Line Driver with $\overline{OE}$	20	4.1	4.6			4.8	5.1	6.5	7.0
CY54/74FCT245T	8-Bit Transceiver with $\overline{OE}$	20	4.1	4.5			4.6	4.9	7.0	7.5
CY54/74FCT257T	Quad 2-input Multiplexers with $\overline{OE}$	16	4.3	5.0			5.0	5.8	6.0	7.0
CY54/74FCT273T	8-Bit Register with Asynchronous Reset	20	5.8	6.5			7.2	8.3	13.0	15.0
CY54/74FCT373T	8-Bit Latch with $\overline{OE}$	20	4.2	5.1			5.2	5.6	8.0	8.5
CY54/74FCT374T	8-Bit Register with $\overline{OE}$	20	5.2	6.2			6.5	7.2	10.0	11.0
CY54/74FCT377T	8-Bit Register with Clock Enable	20	5.2	5.5			7.2	8.3	13.0	15.0
CY54/74FCT399T	Quad 2-input Registers	16	6.1	6.6			7.0	7.5	10.0	11.5
CY54/74FCT480T	Dual 8-Bit Even-Parity Generators/ Checkers	24			5.6	7.0	7.5	9.5	13.0	17.0
CY54/74FCT540T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5
CY54/74FCT541T	8-Bit Buffer/Line Driver with $\overline{OE}$ and Flow-Through Pinout	20	4.3	4.7			4.8	5.1	8.5	9.5
CY54/74FCT543T	8-Bit Latched Transceiver with $\overline{OE}$	24	5.3	6.1			6.5	7.5	8.5	10.0
CY54/74FCT573T	8-Bit Latch with $\overline{OE}$ and Flow-Through Pinout	20	4.2	5.1			5.2	5.6	8.0	8.5
CY54/74FCT574T	8-Bit Register with $\overline{OE}$ and Flow-Through Pinout	20	5.2	6.2			6.5	7.2	10.0	11.0
CY54/74FCT646T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT652T	8-Bit Registered Transceiver with $\overline{OE}$	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT821T	10-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5		
CY54/74FCT823T	9-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5		
CY54/74FCT825T	8-Bit Register with $\overline{OE}$	24	6.0	7.0	7.5	8.5	10.0	11.5		
CY54/74FCT827T	10-Bit Buffer with $\overline{OE}$	24	4.4	5.0	5.0	6.5	8.0	9.0		
CY54/74FCT841T	10-Bit Latch with $\overline{OE}$	24	5.5	6.3	6.5	7.5	9.0	10.0		

Bus Switch

			Propagation Delays (ns)
			Standard
Part Number	Organization	Pins	Com'l
CYBUS3384	10-Bit Bus Switch	24	0.25

FCT2–T Logic Products with Resistor (V_{CC}=5 Volts)

			Propagation Delays (ns)							
			C		B		A		Standard	
Part Number	Organization	Pins	Com'l	Mil	Com'l	Mil	Com'l	Mil	Com'l	Mil
CY54/74FCT2240T	8-Bit Inverting Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.3				4.8	5.1	8.0	9.0
CY54/74FCT2244T	8-Bit Buffer/Line Driver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.8	5.1	6.5	7.0
CY54/74FCT2245T	8-Bit Transceiver with $\overline{OE}$ and 25Ω Resistor	20	4.1				4.6	4.9	7.0	7.5
CY54/74FCT2257T	Quad 2-input Multiplexers with $\overline{OE}$ and 25Ω Resistor	16	4.3				5.0	5.8	6.0	7.0
CY54/74FCT2373T	8-Bit Latch with $\overline{OE}$ and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5
CY54/74FCT2374T	8-Bit Register with $\overline{OE}$ and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0
CY54/74FCT2541T	8-Bit Buffer/Line Driver with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.1	4.6			4.8	5.1	8.0	9.0
CY54/74FCT2543T	8-Bit Latched Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.5	6.1			6.5	7.5	8.5	10.0
CY54/74FCT2573T	8-Bit Latch with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	4.7	5.1			5.2	5.6	8.0	8.5
CY54/74FCT2574T	8-Bit Register with $\overline{OE}$, Flow-Through Pinout and 25Ω Resistor	20	5.2	6.0			6.5	7.2	10.0	11.0
CY54/74FCT2646T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT2648T	8-Bit Inverting Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT2652T	8-Bit Registered Transceiver with $\overline{OE}$ and 25Ω Resistor	24	5.4	6.0			6.3	7.7	9.0	11.0
CY54/74FCT2827T	10-Bit Buffer with $\overline{OE}$ and 25Ω Resistor	24	4.4	5.0	5.0	6.5	8.0	9.0		

Notes:

The above specifications are for the Commercial temperature range of 0°C to 70°C and Military temperature range of −55°C to +125°C. Contact your local sales office for more information.

Commercial grade product is available in plastic. Military grade product is available in CERDIP and LCC.

All power supplies are V_{CC} = 5V ± 5% (V_{CC} = 5V ± 10% for Military).

PRODUCT LINE CROSS REFERENCE

AMD	CYPRESS
AM29C818A	CY29FCT818T/AT/BT/CT
AM29C821	CY74FCT821AT/BT/CT
AM29C823	CY74FCT823AT/BT/CT
AM29C825	CY74FCT825AT/BT/CT
AM29C827	CY74FCT827AT/BT/CT
AM29C841	CY74FCT841AT/BT/CT

HARRIS	CYPRESS
CD74FCT2952A	CY29FCT52AT
CD74FCT29520A	CY29FCT520AT
CD74FCT240	CY74FCT240T
CD74FCT244	CY74FCT244T
CD74FCT245	CY74FCT245T
CD74FCT273	CY74FCT273T
CD74FCT373	CY74FCT373T
CD74FCT374	CY74FCT374T
CD74FCT377	CY74FCT377T
CD74FCT540	CY74FCT540T
CD74FCT541	CY74FCT541T
CD74FCT543	CY74FCT543T
CD74FCT573	CY74FCT573T
CD74FCT574	CY74FCT574T
CD74FCT646	CY74FCT646T
CD74FCT648	CY74FCT648T
CD74FCT652	CY74FCT652T
CD74FCT821A	CY74FCT821AT
CD74FCT823A	CY74FCT823AT
CD74FCT827A	CY74FCT827AT
CD74FCT841A	CY74FCT841AT

IDT	CYPRESS
IDT29FCT52AT/BT/CT	CY29FCT52AT/BT/CT
IDT29FCT520AT/BT/CT	CY29FCT520AT/BT/CT
IDT74FCT138T/AT/CT	CY74FCT138T/AT/CT
IDT74FCT157T/AT/CT	CY74FCT157T/AT/CT
IDT74FCT163T/AT/CT	CY74FCT163T/AT/CT
IDT74FCT191T/AT	CY74FCT191T/AT
IDT74FCT240T/AT/CT	CY74FCT240T/AT/CT
IDT74FCT244T/AT/CT	CY74FCT244T/AT/CT
IDT74FCT245T/AT/CT	CY74FCT245T/AT/CT
IDT74FCT257T/AT/CT	CY74FCT257T/AT/CT
IDT74FCT273T/AT/CT	CY74FCT273T/AT/CT
IDT74FCT373T/AT/CT	CY74FCT373T/AT/CT
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IDT74FCT827AT/BT/CT	CY74FCT827AT/BT/CT
IDT74FCT841AT/BT/CT	CY74FCT841AT/BT/CT
IDT74FBT2240T/AT/CT	CY74FCT2240AT/CT
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IDT74FBT2373T/AT/CT	CY74FCT2373AT/CT
IDT74FBT2827AT/BT/CT	CY74FCT2827AT/BT/CT

NATIONAL	CYPRESS
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74FCT240/A	CY74FCT240T/AT
74FCT244/A	CY74FCT244T/AT
74FCT245/A	CY74FCT245T/AT
74FCT273/A	CY74FCT273T/AT
74FCT373/A	CY74FCT373T/AT
74FCT374/A	CY74FCT374T/AT
74FCT377/A	CY74FCT377T/AT
74FCT543/A	CY74FCT543T/AT
74FCT573/A	CY74FCT573T/AT
74FCT574/A	CY74FCT574T/AT
74FCT646/A	CY74FCT646T/AT
74FCT821A/B	CY74FCT821AT/BT
74FCT823A/B	CY74FCT823AT/BT
74FCT825A/B	CY74FCT825AT/BT
74FCT827A/B	CY74FCT827AT/BT
74FCT841A/B	CY74FCT841AT/BT

PERICOM (PIONEER)	CYPRESS
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PI74FCT244T/AT/CT	CY74FCT244T/AT/CT
PI74FCT245T/AT/CT	CY74FCT245T/AT/CT
PI74FCT273T/AT/CT	CY74FCT273T/AT/CT
PI74FCT373T/AT/CT	CY74FCT373T/AT/CT
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PI74FCT2827T/AT/CT	CY74FCT2827AT/BT/CT
PI5C3384A	CYBUS3384

QUALITY	CYPRESS
QS29FCT52AT/BT/CT	CY29FCT52AT/BT/CT
QS29FCT520AT/BT/CT	CY29FCT520AT/BT/CT
QS74FCT138T/AT/CT	CY74FCT138T/AT/CT
QS74FCT157T/AT/CT	CY74FCT157T/AT/CT
QS74FCT158T/AT/CT	CY74FCT158T/AT/CT
QS74FCT163T/AT/CT	CY74FCT163T/AT/CT
QS74FCT191T/AT/CT	CY74FCT191T/AT/CT
QS74FCT240T/AT/CT	CY74FCT240T/AT/CT
QS74FCT244T/AT/CT	CY74FCT244T/AT/CT
QS74FCT245T/AT/CT	CY74FCT245T/AT/CT
QS74FCT257T/AT/CT	CY74FCT257T/AT/CT
QS74FCT273T/AT/CT	CY74FCT273T/AT/CT
QS74FCT373T/AT/CT	CY74FCT373T/AT/CT

PRODUCT LINE CROSS REFERENCE

QUALITY	CYPRESS
QS74FCT374T/AT/CT	CY74FCT374T/AT/CT
QS74FCT377T/AT/CT	CY74FCT377T/AT/CT
QS74FCT540T/AT/CT	CY74FCT540T/AT/CT
QS74FCT541T/AT/CT	CY74FCT541T/AT/CT
QS74FCT543T/AT/CT	CY74FCT543T/AT/CT
QS74FCT573T/AT/CT	CY74FCT573T/AT/CT
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QS74FCT2240T/AT/CT	CY74FCT2240AT/CT
QS74FCT2244T/AT/CT	CY74FCT2244AT/CT
QS74FCT2245T/AT/CT	CY74FCT2245AT/CT
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QS74FCT2646T/AT/CT	CY74FCT2646AT/CT
QS74FCT2648T/AT/CT	CY74FCT2648AT/CT
QS74FCT2652T/AT/CT	CY74FCT2652AT/CT
QS74FCT2827AT/BT/CT	CY74FCT2827AT/BT/CT
QS3384	CYBUS3384

PERFORMANCE TO CYPRESS CROSS REFERENCE

1. Change the prefix from P to CY
2. Device number/speed code remains the same.
3. Use the following package codes:

Performance	Cypress	Comments
P	P	Same
D	D	Same
L	L	Same
SO	SO	Same
S	Q	Different

4. Use the suffix C for Commercial devices or MB for Military devices.

PACKAGE DESIGNATOR CROSS REFERENCE

AMD	CYPRESS
D	D
L	L
P	P
S	SO

IDT	CYPRESS
D	D
L	L
P	P
SO	SO

NATIONAL	CYPRESS
D	D
L	L
P	P
S	SO

PERICOM (PIONEER)	CYPRESS
P	P
Q	Q
S	SO

PHILIPS	CYPRESS
D	SO
N	P

QUALITY	CYPRESS
D	D
L	L
P	P
Q	Q
SO	SO

Document #: 38–00352

SECTION CONTENTS

FCT–T

Bus Switch

CY29FCT52T
8-BIT REGISTERED TRANSCEIVER

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F and AM2952 Logic**
- **FCT-C speed at 6.3ns max. (Com'l) FCT-B speed at 7.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

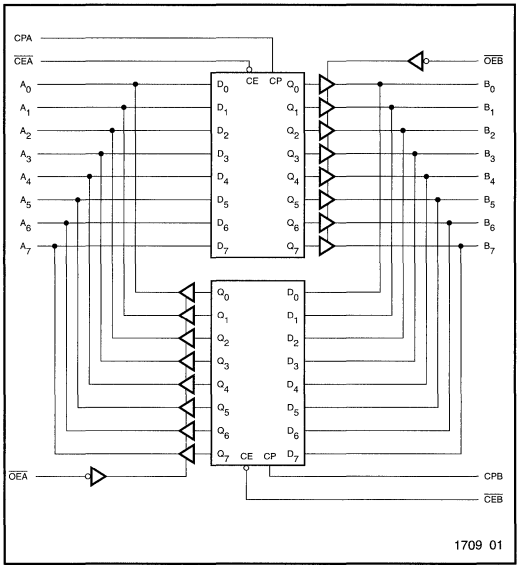
2

DESCRIPTION

The 'FCT52T has two 8-bit back-to-back registers that store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register.

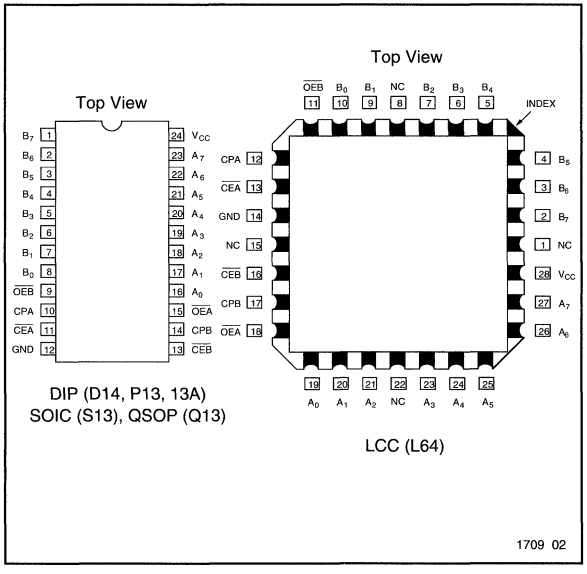
Both A outputs and B outputs are guaranteed to sink 64mA. The 'FCT52T is non-inverting.

FUNCTIONAL BLOCK DIAGRAM



1709 01

PIN CONFIGURATIONS



1709 02

REGISTERED FUNCTION TABLE

Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	⎍	L	L	Load Data
H	⎍	L	H	

1709 Tbl 01

OUTPUT CONTROL

$\overline{OE}$	Internal Q	Y-Output	Function
H	X	Z	Disable Outputs
L	L	L	Enable Outputs
L	H	H	

1709 Tbl 02

PIN DESCRIPTION

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high impedence state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high impedence state.

1709 Tbl 03

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1709 Tbl 04

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1709 Tbl 05

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1709 Tbl 06

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1709 Tbl 07

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1709 Tbl 08

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEA}$ or $\overline{OEB}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	2.0	4.0	mA	V_{CC} = MAX, f_0 = 10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEA}$ or $\overline{OEB}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.5	6.0	mA	V_{CC} = MAX, f_0 = 10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEA}$ or $\overline{OEB}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.3	7.8[4]	mA	V_{CC} = MAX, f_0 = 10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OEA}$ or $\overline{OEB}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.5	16.8[4]	mA	V_{CC} = MAX, f_0 = 10 MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OEA}$ or $\overline{OEB}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1709 Tbl 09

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT52AT				'FCT52BT				'FCT52CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to B_n, A_n	2.0	11.0	2.0	10.0	2.0	8.0	2.0	7.5	2.0	7.3	2.0	6.3	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	13.0	1.5	10.5	1.5	8.5	1.5	8.0	1.5	8.0	1.5	7.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	1.5	10.0	1.5	10.0	1.5	8.0	1.5	7.5	1.5	7.5	1.5	6.5	ns	1,7,8

Notes:

1709 Tbl 10

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

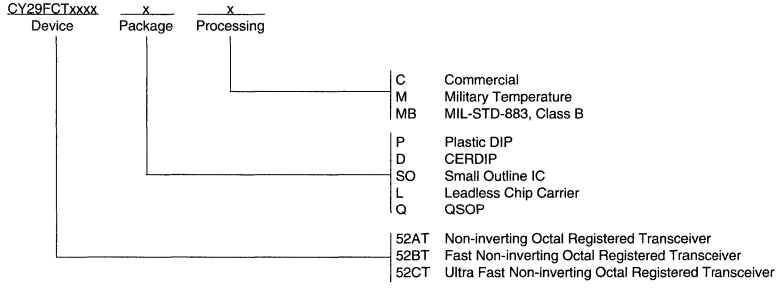
Symbol	Parameter	'FCT52AT				'FCT52BT				'FCT52CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW, A_n, B_n to CPA, CPB	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, A_n, B_n to CPA, CPB	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH[3] or LOW, CPA or CPB	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	ns	5

Note:

1709 Tbl 11

3. This parameter is guaranteed but not tested.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1709 03

CY29FCT520T
MULTILEVEL PIPELINE REGISTER

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F Logic and AM29520**
- **FCT-C speed at 6.0ns max. (Com'l) FCT-B speed at 7.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Single and Dual Pipeline Operation Modes**
- **Multiplexed Data Inputs and Outputs**

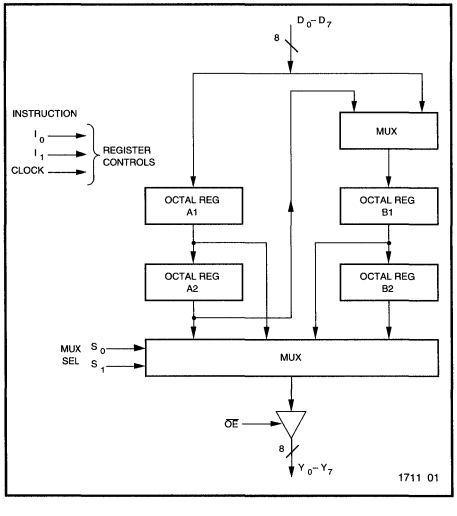
DESCRIPTION

The 'FCT520T is a multi-level 8-bit wide pipeline register. The device consists of 4 registers A1, A2, B1 and B2 which are configured by the instruction inputs I_0, I_1 as a single 4-level pipeline or as two 2-level pipelines. The contents of any register may be read at the multiplexed output at any time by using the mux-selection controls S_0 and S_1.

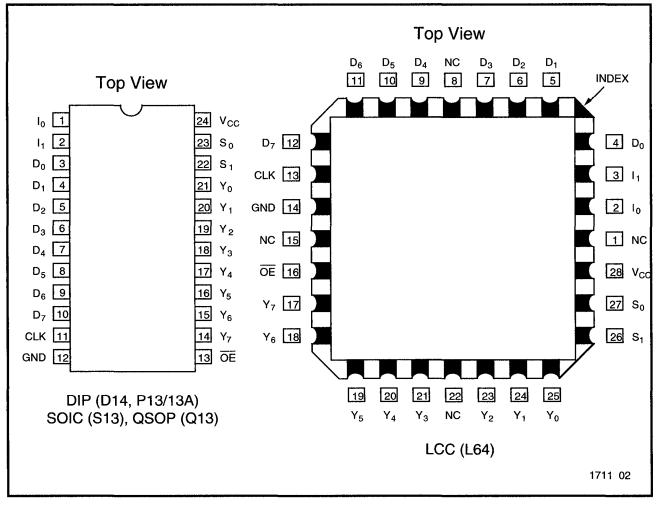
The pipeline register is positive edge triggered and data is shifted by the rising edge of the clock input. Instruction I = 0 selects the 4-level pipeline mode. Instruction I = 1 selects the 2-level B pipeline while I = 2 selects the 2-level A pipeline. I = 3 is the HOLD instruction; no shifting is performed by the clock in this mode.

In the 2-level operation mode, the 'FCT520T data is shifted from level 1 to level 2 and new data is loaded into level 1.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1711 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1711 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1711 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1711 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1711 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, Outputs Open, f_1 = 0, V_{IN} = 3.4V[2]
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1711 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

OUTPUT SELECTION MUX TABLE

S_1	S_0	Output
1	1	A1
1	0	A2
0	1	B1
0	0	B2

1711 Tbl 07

AC CHARACTERISTICS

Symbol	Parameter	'FCT520AT				Units	Fig. No.*
		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Clock to Data Output	2.0	16.0	2.0	14.0	ns	5
t_{PLH} t_{PHL}	S0, S1 To Data Output	2.0	15.0	2.0	13.0	ns	5
t_S	Setup Time Input Data to Clock	6.0	—	5.0	—	ns	5
t_H	Hold Time Input Data to Clock	2.0	—	2.0	—	ns	5
t_S	Setup Time Instruction (Reg. Enable) to Clock	6.0	—	5.0	—	ns	5
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0	—	2.0	—	ns	5
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	13.0	1.5	12.0	ns	8, 7
t_{PZH} t_{PZL}	Output Enable Time	1.5	16.0	1.5	15.0	ns	8, 7
$t_W(H)$ $t_W(L)$	Clock Pulse Width, High or Low	8.0	—	7.0	—	ns	5

1711 Tbl 09

Notes:

* See "Parameter Measurement Information" in the General Information Section.

AC CHARACTERISTICS

Symbol	Parameter	'FCT520BT				'FCT520CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Clock to Data Output	2.0	8.0	2.0	7.5	2.0	7.0	2.0	6.0	ns	5
t_{PLH} t_{PHL}	S0, S1 To Data Output	2.0	8.0	2.0	7.5	2.0	7.0	2.0	6.0	ns	5
t_S	Setup Time Input Data to Clock	2.8	—	2.5	—	2.8	—	2.5	—	ns	5
t_H	Hold Time Input Data to Clock	2.0	—	2.0	—	2.0	—	2.0	—	ns	
t_S	Setup Time Instruction (Reg. Enable) to Clock	4.5	—	4.0	—	4.5	—	4.0	—	ns	
t_H	Hold Time Instruction (Reg. Enable) to Clock	2.0	—	2.0	—	2.0	—	2.0	—	ns	
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	6.0	1.5	6.0	ns	8, 7
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.0	1.5	7.5	1.5	7.0	1.5	6.0	ns	8, 7
$t_W(H)$ $t_W(L)$	Clock Pulse Width, High or Low	6.0	—	5.5	—	6.0	—	5.5	—	ns	5

1711 Tbl 10

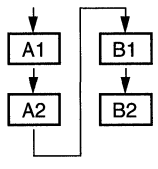
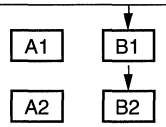
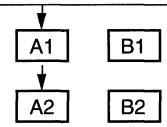
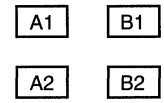
Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.

AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

PIPELINE INSTRUCTION TABLE

I = 0	I = 1	I = 2	I = 3
$I_1 = 0$, $I_0 = 0$	$I_1 = 0$ $I_0 = 1$	$I_1 = 1$ $I_0 = 0$	$I_1 = 1$ $I_0 = 1$
			
Single 4-level	Dual 2-level		Hold

ORDERING INFORMATION

CY29FCT xxxx x x

Device type / Package / Processing

C	Commercial
M	Military Temperature
MB	MIL-STD-883, Class B
P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
Q	QSOP
520AT	Fast Multi-level PipelineRegister
520BT	Ultra Fast Multi-level PipelineRegister
520CT	Fastest Multi-level PipelineRegister

1711 03

CY29FCT818T
DIAGNOSTIC SCAN REGISTER

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F Logic and AM29818**
- **FCT-C speed at 6.0ns max. (Com'l) FCT-B speed at 7.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 20 mA (Mil) 15 mA Source Current (Com'l), 3 mA (Mil)**
- **8-Bit Pipeline and Shadow Register**

2

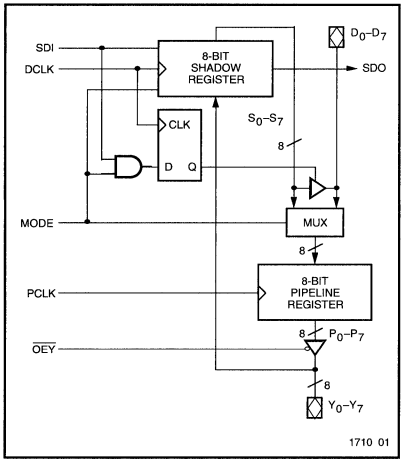
DESCRIPTION

The 'FCT818T contain a high speed 8-bit general-purpose data pipeline register and a high speed 8-bit shadow register. The general-purpose register can be used in an 8-bit wide data path for a normal system application. The shadow register is designed for applications, such as diagnostics in sequential circuits, where it is desirable to load known data at a specific location in the circuit and to read the data at that location.

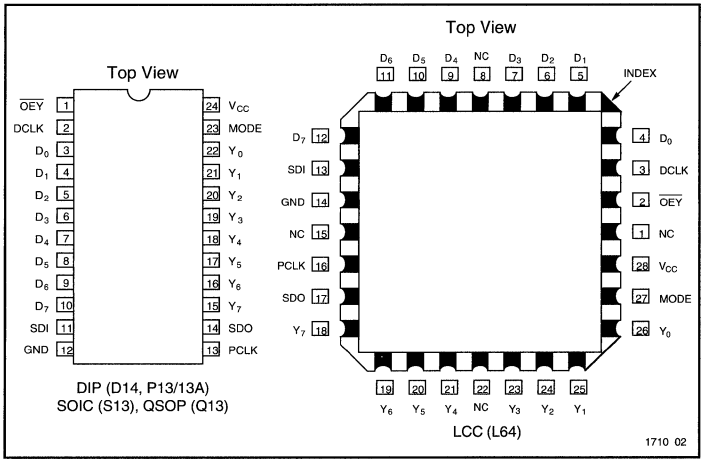
The shadow registers can load data from the output of the 'FCT818T, and can be used as a right-shift register with bit-serial input SDI and output SDO, using DCLK. The data register input is multiplexed to enable loading from the shadow register or from the data input pins using PCLK. Note that data can be loaded simultaneously from the shadow register to the pipeline register, and from the pipeline register to the shadow register provided set-up and hold time requirements are satisfied with respect to the two independent clock inputs.

In a typical application, the general-purpose register in the 'FCT818T replaces an 8-bit data register in the normal data path of a system. The shadow register is placed in an auxiliary bit-serial loop which is used for diagnostics. During diagnostic operation, data is shifted serially into the shadow register, then transferred to the general-purpose register to load a known value into the data path. To read the contents at that point in the data path, the data is transferred from the data register into the shadow register, then shifted serially in the auxiliary diagnostic loop to make it accessible to the diagnostics controller. This data is then compared with the expected value to diagnose faulty operation of the sequential circuit.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



The contents of the shadow register can also be output by enabling the 8-bit wide D input/output port. In an application such as micro-program testing, the microinstruction register is formed using the general-purpose registers of 'FCT818T devices with cascaded shadow registers. To modify the microinstruction register, the corrected instruction word is shifted serially into the shadow registers and then transferred into the data registers. This word is also loaded easily into the Writeable Control Store (WCS) by enabling the D output from the shadow registers.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –3mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 20mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 24mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				5	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1710 Tbl 01

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1710 Tbl 02

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1710 Tbl 03

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min.	Max.
Military	–55°C	+125°C
Commercial	0°C	+70°C

1710 Tbl 04

Supply Voltage (V_{CC})	Min.	Max.
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1710 Tbl 05

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[1]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, Outputs Open, f_1 = 0, V_{IN} = 3.4V
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OEY}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[c]		5.3	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEY}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			7.3	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OEY}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
			17.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, $\overline{OEY}$ = GND, f_1 = 5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			30.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits and Four Controls Toggling, $\overline{OEY}$ = GND, f_1 = 5MHz, V_{IN} = 3.4V or V_{IN} = GND

1710 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	'FCT818T				'FCT818AT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PD}	PCLK TO Yx	—	18	—	13	—	12	—	9	ns	5
	MODE to SDO	—	18	—	16	—	18	—	16	ns	6
	SDI to SDO	—	18	—	16	—	18	—	15	ns	3
	DCLK to SDO	—	30	—	25	—	30	—	25	ns	5
t_S	Dx to PCLK	10	—	8	—	6	—	4	—	ns	
	MODE to PCLK	15	—	15	—	15	—	15	—	ns	
	Yx to DCLK	5	—	5	—	5	—	5	—	ns	
	MODE to DCLK	12	—	12	—	12	—	12	—	ns	4
	SDI to DCLK	10	—	10	—	10	—	10	—	ns	
	DCLK to PCLK	15	—	15	—	15	—	15	—	ns	
	PCLK to DCLK	45	—	40	—	45	—	40	—	ns	
t_H	Dx to PCLK	2	—	2	—	2	—	2	—	ns	
	MODE to PCLK	0	—	0	—	0	—	0	—	ns	
	Yx to DCLK	5	—	5	—	5	—	5	—	ns	4
	MODE to DCLK	5	—	2	—	5	—	2	—	ns	
	SDI to DCLK	0	—	0	—	0	—	0	—	ns	
t_{PLZ}	$\overline{OEY}$ to Yx	—	20	—	15	—	20	—	15	ns	7
	DCLK to Dx	—	45	—	45	—	45	—	45	ns	5
t_{PHZ}	$\overline{OEY}$ to Yx	—	30	—	25	—	30	—	25	ns	8
	DCLK to Dx	—	90	—	85	—	90	—	80	ns	5
t_{PZL}	$\overline{OEY}$ to Yx	—	20	—	15	—	20	—	15	ns	7
	DCLK to Dx	—	35	—	30	—	35	—	25	ns	5
t_{PZH}	$\overline{OEY}$ to Yx	—	20	—	15	—	20	—	15	ns	8
	DCLK to Dx	—	30	—	25	—	30	—	25	ns	5
t_W	PCLK (High and Low)	15	—	15	—	15	—	10	—	ns	5
	DCLK (High and Low)	25	—	25	—	25	—	15	—	ns	5

1710 Tbl 07

Notes:
AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
*See "Parameter Measurement Information" in the General Information Section.

AC CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter	'FCT818BT				'FCT818CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{PD}	PCLK TO Yx	—	9.0	—	7.5	---	7.6	---	6.0	ns	5
	MODE to SDO	—	10.5	—	9.0	---	8.9	---	7.2	ns	6
	SDI to SDO	—	10.5	—	9.0	---	8.9	---	7.1	ns	3
	DCLK to SDO	—	10.5	—	9.0	---	8.9	---	7.2	ns	5
t_S	Dx to PCLK	4.5	—	3.0	—	3.0	---	2.0	---	ns	4
	MODE to PCLK	6.5	—	5.0	—	5.0	---	3.5	---	ns	
	Yx to DCLK	4.5	—	3.0	—	3.0	---	2.0	---	ns	
	MODE to DCLK	6.5	—	5.0	—	5.0	---	3.5	---	ns	
	SDI to DCLK	6.5	—	5.0	—	5.0	---	3.5	---	ns	
	DCLK to PCLK	6.5	—	5.0	—	5.0	---	3.5	---	ns	
	PCLK to DCLK	12.5	—	11.0	—	11.0	---	8.5	---	ns	
t_H	Dx to PCLK	2	—	2	—	2.0	---	1.5	---	ns	4
	MODE to PCLK	0	—	0	—	0	---	0	---	ns	
	Yx to DCLK	3	—	2	—	3.0	---	1.5	---	ns	
	MODE to DCLK	3	—	2	—	3.0	---	1.5	---	ns	
	SDI to DCLK	0	—	0	—	0	---	0	---	ns	
t_{PLZ}	$\overline{OEY}$ to Yx	—	8.5	—	7.0	---	7.0	---	5.5	ns	7
	DCLK to Dx	—	8.5	—	7.0	---	7.0	---	5.5	ns	5
t_{PHZ}	$\overline{OEY}$ to Yx	—	10.5	—	9.0	---	9.0	---	8.0	ns	8
	DCLK to Dx	—	10.5	—	9.0	---	9.0	---	8.0	ns	5
t_{PZL}	$\overline{OEY}$ to Yx	—	11.5	—	10.0	---	10.0	---	8.0	ns	7
	DCLK to Dx	—	11.5	—	10.0	---	10.0	---	9.0	ns	5
t_{PZH}	$\overline{OEY}$ to Yx	—	11.5	—	10.0	---	10.0	---	8.5	ns	8
	DCLK to Dx	—	12.5	—	11.0	---	11.0	---	9.0	ns	5
t_W	PCLK (High and Low)	7.0	—	6.0	—	6.0	---	5.0	---	ns	5
	DCLK (High and Low)	7.0	—	6.0	—	6.0	---	5.0	---	ns	5

1710 Tbl 08

Notes:
AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
*See "Parameter Measurement Information" in the General Information Section.

FUNCTION TABLE

Inputs				Outputs			Operation
MODE	SDI	DCLK	PCLK	SDO	Shadow Register	Pipeline Register	
L	X	⌐¬	X	S_7	$S_0 \leftarrow SDI$ $S_i \leftarrow S_{i-1}$	NA	Serial Shift; D_7–D_0 Output Disabled
L	X	X	⌐¬	S_7	NA	$P_i \leftarrow D_i$	Load Pipeline Register from Data Input
H	L	⌐¬	X	L	$S_i \leftarrow Y_i$	NA	Load Shadow Register from Y Output
H	H	⌐¬	X	H	Hold	NA	Hold Shadow Register; D_7–D_0 Output Enabled
H	X	X	⌐¬	SDI	NA	$P_i \leftarrow S_i$	Load Pipeline Register from Shadow Register

Note: NA = Not Applicable

1710 Tbl 09

ORDERING INFORMATION

CY29FCT — xxxxx (Device type) — x (Package) — x (Processing)

Processing	
C	Commercial
M	Military Temperature
MB	MIL-STD-883, Class B
Package	
P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
Q	QSOP
Device type	
818T	Diagnostic Scan Register
818AT	Fast Diagnostic Scan Register
818BT	Ultra Fast Diagnostic Scan Register
818CT	Ultra Fast Diagnostic Scan Register

1710 03

CY54/74FCT138T
1-OF-8 DECODER

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.0ns max. (Com'l) FCT-A speed at 5.8ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Dual 1-Of-8 Decoder with Enables**

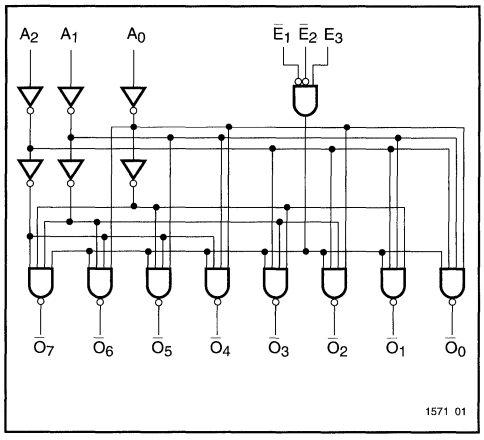
2

DESCRIPTION

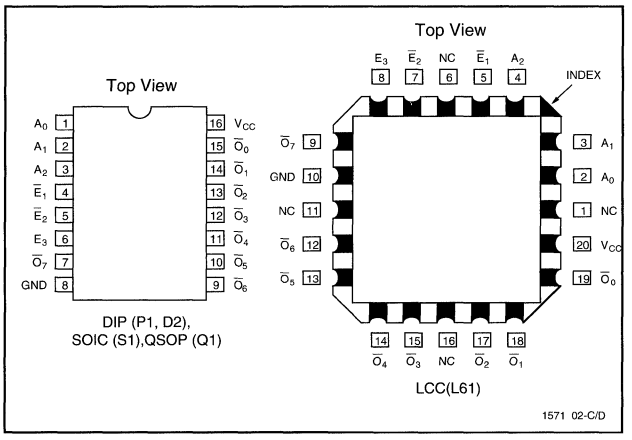
The 'FCT138T are 1-of-8 decoders. The 'FCT138T accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\overline{O}_0 - \overline{O}_7$). The 'FCT138T features three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3).

All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'FCT138T devices and one inverter.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1571 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1571 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1571 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1571 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1571 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.3	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.5	mA	V_{CC} = MAX, f_1 = 10MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3, One Output Toggling, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.5	mA	V_{CC} = MAX, f_1 = 10MHz, 50% Duty Cycle, Outputs Open, Toggle $\overline{E}_1$, $\overline{E}_2$ or E_3, One Output Toggling, V_{IN} = 3.4V or V_{IN} = GND

1571 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + I_{CC}D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Output Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level, L=LOW Voltage Level, X=Don't Care

1571 Tbl 07

AC CHARACTERISTICS

Sym	Parameter	'FCT138T				'FCT138AT				'FCT138CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Prop Delay A_0 to $\overline{O}_n$	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	1.5	6.0	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.1	1.5	5.0	ns	1, 5
t_{PLH} t_{PHL}	Prop Delay E_3 to $\overline{O}_n$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	1.5	6.1	1.5	5.0	ns	1, 5

1571 Tbl 08

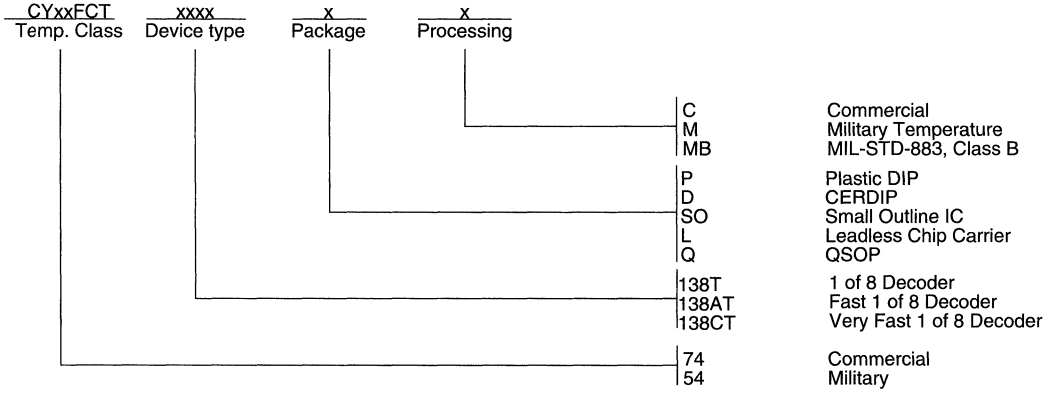
Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

DEFINITION OF FUNCTIONAL TERMS

PIN Names	Description
$A_0 - A_2$	Address Inputs
$\overline{E}_1 - \overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)

1571 Tbl 08

ORDERING INFORMATION



1571 03

CY54/74FCT157T
CY54/74FCT158T
QUAD 2-INPUT MULTIPLEXERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.3ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

2

DESCRIPTION

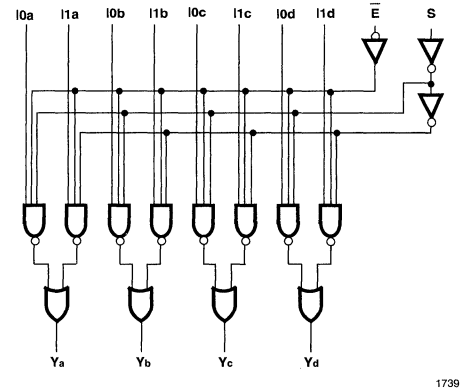
The 'FCT157T and 'FCT158T are quad 2-input multiplexers which select 4 bits of data from two sources under the control of a common data Select input (S). The Enable input $\overline{E}$ is active-low. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 'FCT157T and 'FCT158T. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the sixteen different functions of two variables with one variable common.

These devices are logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The outputs of the 'FCT157T are Non-Inverting whereas the 'FCT158T has inverting outputs.

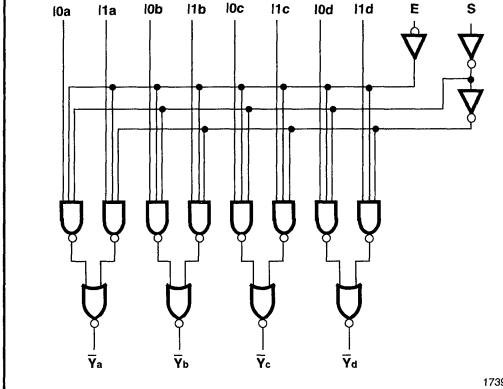
FUNCTIONAL BLOCK DIAGRAM

'FCT157T



1739 01

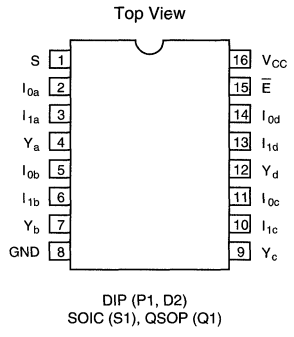
'FCT158T

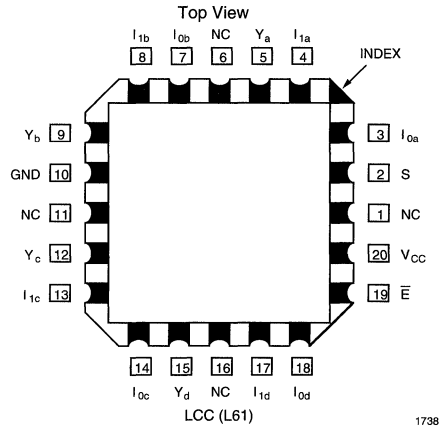


1739 02

PIN CONFIGURATIONS

'FCT157T

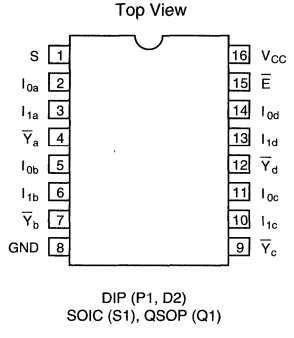


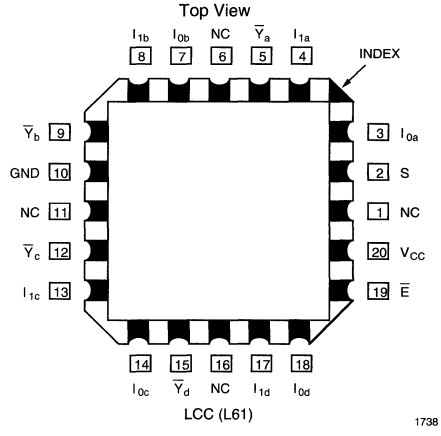


1738 03

PIN CONFIGURATIONS

'FCT158T

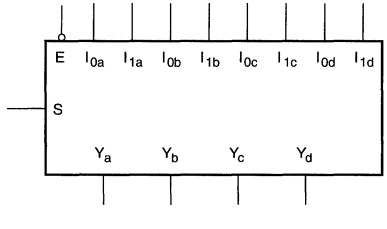




1738 04

LOGIC SYMBOL

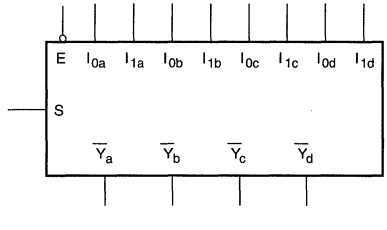
'FCT157T



1738 05

LOGIC SYMBOL

'FCT158T



1738 06

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1739 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1739 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1739 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1739 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1739 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[1]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		1.7	4.0[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.7	8.0[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1738 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE — 'FCT157T

Enable	Select Inputs	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

1738 Tbl 07

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance (OFF) state

FUNCTION TABLE — 'FCT158T

Enable	Select Inputs	Data Inputs		Output
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	X	L	H
L	L	X	H	L
L	H	L	X	H
L	H	H	X	L

1738 Tbl 08

PIN DESCRIPTIONS

Pin Names	Description
S	Common Select Input
$\overline{E}$	Enable Input (Active LOW)
$I_{0A} - I_{0D}$	Data Inputs from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Y_A - Y_D$	Non-Inverted Output
$\overline{Y}_A - \overline{Y}_D$	Inverted Output

1738 Tbl 09

AC CHARACTERISTICS ('FCT157T)

Symbol	Parameter	'FCT157T				'FCT157AT				'FCT157CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH}, t_{PHL}	Propagation Delay I_n to Y	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Y	1.5	12.0	1.5	10.5	1.5	7.4	1.5	6.0	1.5	5.9	1.5	4.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	1.5	6.0	1.5	5.2	ns	1, 3

1738 Tbl 10

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

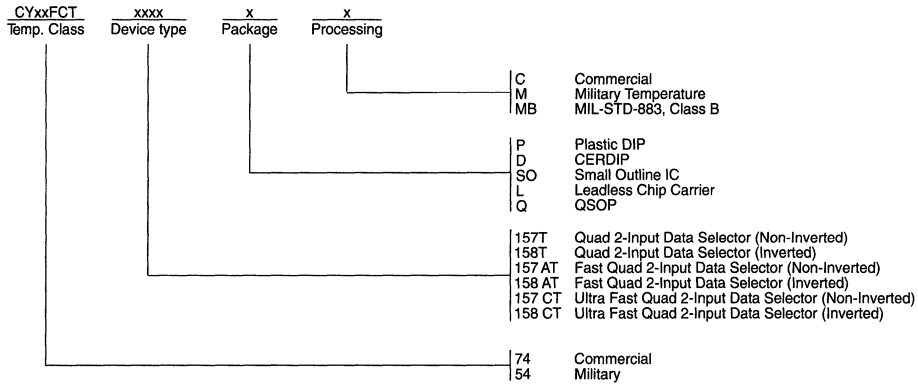
AC CHARACTERISTICS ('FCT158T)

Symbol	Parameter	'FCT158T				'FCT158AT				'FCT158CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay I_n to Y	1.5	7.5	1.5	6.5	1.5	6.3	1.5	5.5	1.5	5.5	1.5	4.8	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Y	1.5	12.5	1.5	11.0	1.5	7.9	1.5	6.5	1.5	6.4	1.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay S to Y	1.5	12.5	1.5	11.0	1.5	8.6	1.5	7.5	1.5	6.5	1.5	5.7	ns	1, 2

1738 Tbl 11

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1739 05

CY54/74FCT163T
4-BIT BINARY COUNTER

FEATURES

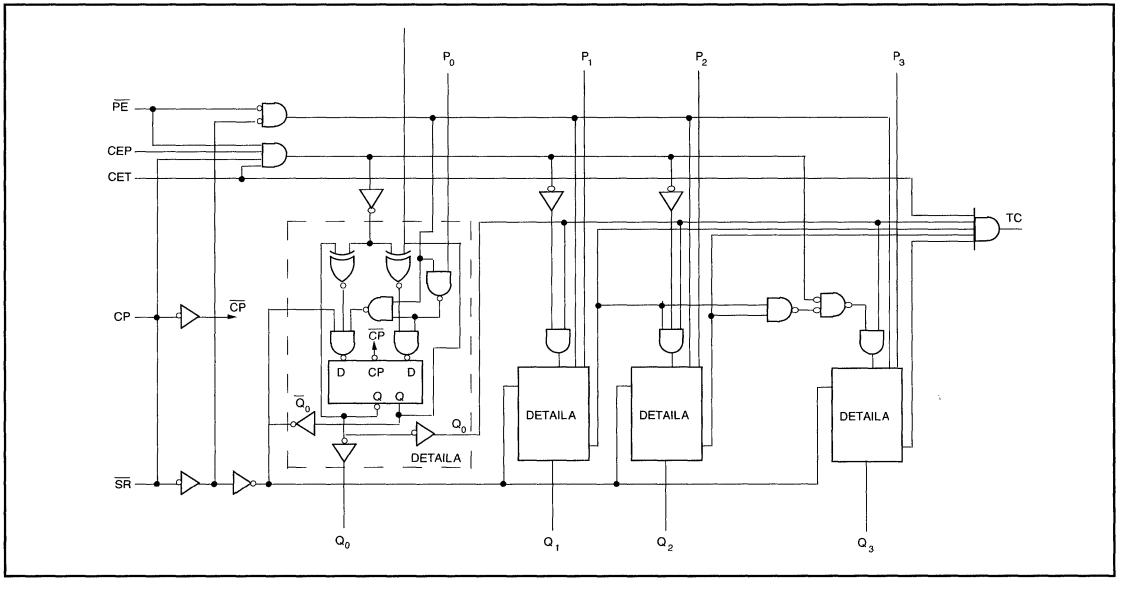
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.8ns max. (Com'l)**
  FCT-A speed at 7.2ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil)**
  15 mA Source Current (Com'l), 12 mA (Mil)

2

DESCRIPTION

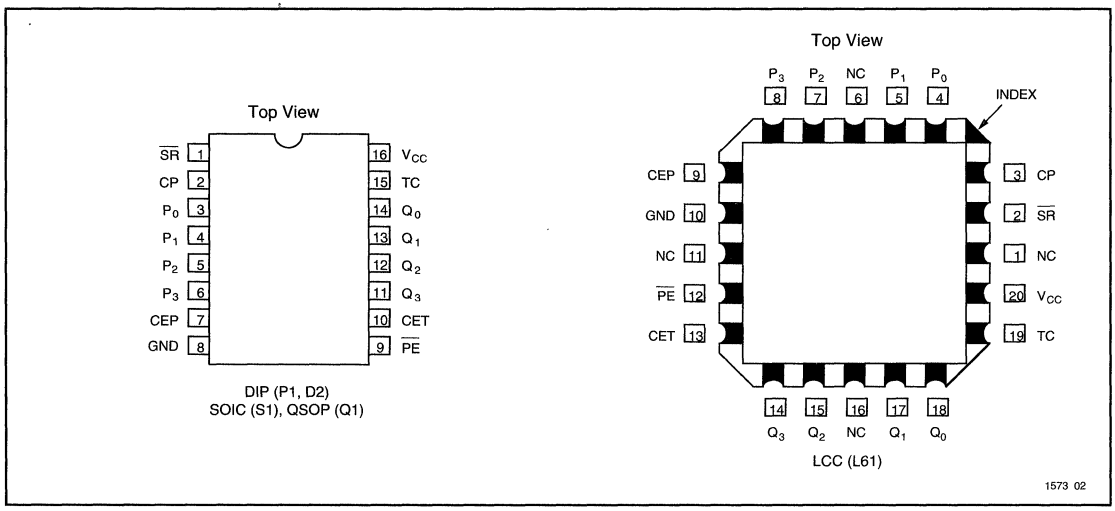
The 'FCT163T is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The 'FCT163T has a Synchronous Reset input that override counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



1573 01

PIN CONFIGURATIONS



DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{SR}$	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

1573 Tbl 01

TRUTH TABLE

$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge(s)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Incremental)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

1573 Tbl 02

Note:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1573 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1573 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1573 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1573 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1573 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)[2]	0.2	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, $\overline{CEP}$ = CET = $\overline{PE}$ = GND, $\overline{SR}$ = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA/	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{SR}$ = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{SR}$ = V_{CC} V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{SR}$ = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bit Toggling at f_1 = 5MHz, CEP = CET = $\overline{PE}$ = GND, $\overline{SR}$ = V_{CC} V_{IN} = 3.4V or V_{IN} = GND

1573 Tbl 08

Notes:

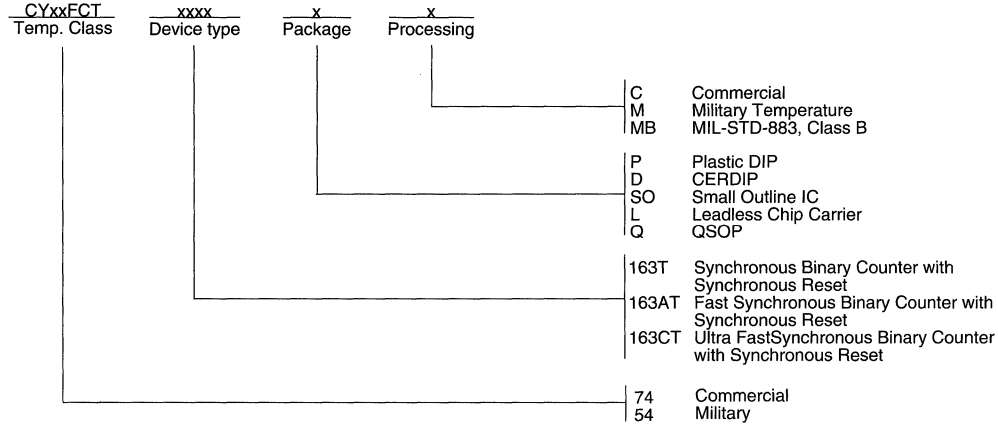
1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT163T				'FCT163AT				'FCT163CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP TO Q_n ($\overline{PE}$ Input High)	2.0	11.5	2.0	11.0	2.0	7.5	2.0	7.2	1.5	6.1	1.5	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP TO Q_N ($\overline{PE}$ Input Low)	2.0	10.0	2.0	9.5	2.0	6.5	2.0	6.2	1.5	5.5	1.5	5.2	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CP TO TC	2.0	16.5	2.0	15.0	2.0	10.8	2.0	9.8	1.5	8.7	1.5	7.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay CET TO TC	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	1.5	4.8	1.5	4.4	ns	1, 5
$t_S(H)$ $t_S(L)$	Setup Time HIGH or LOW P_n to CP	5.5	—	5.0	—	4.5	—	4.0	—	3.9	—	3.5	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW P_n to CP	2.0	—	1.5	—	2.0	—	1.5	—	2.0	—	1.5	—	ns	4
$t_{SU}(H)$ $t_{SU}(L)$	Setup Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	13.5	—	11.5	—	11.5	—	9.5	—	9.0	—	7.6	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.0	—	ns	4
$t_{SU}(H)$ $t_{SU}(L)$	Setup Time HIGH or LOW CEP or CET to CP	13.0	—	11.5	—	11.0	—	9.5	—	8.8	—	7.6	—	ns	4
$t_H(H)$ $t_H(L)$	Hold Time HIGH or LOW CEP or CET to CP	0	—	0	—	0	—	0	—	0	—	0	—	ns	4
$t_W(H)$ $t_W(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0	—	5.0	—	4.0[2]	—	4.0[2]	—	4.0[2]	—	4.0[2]	—	ns	5
$t_W(H)$ $t_W(L)$	Clock Pulse Width (Count) HIGH or LOW	8.0	—	7.0	—	7.0	—	6.0	—	6.0	—	5.0	—	ns	5

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. This parameter is guaranteed but not tested.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1573 03

CY54/74FCT191T
4-BIT UP/DOWN BINARY COUNTER

FEATURES

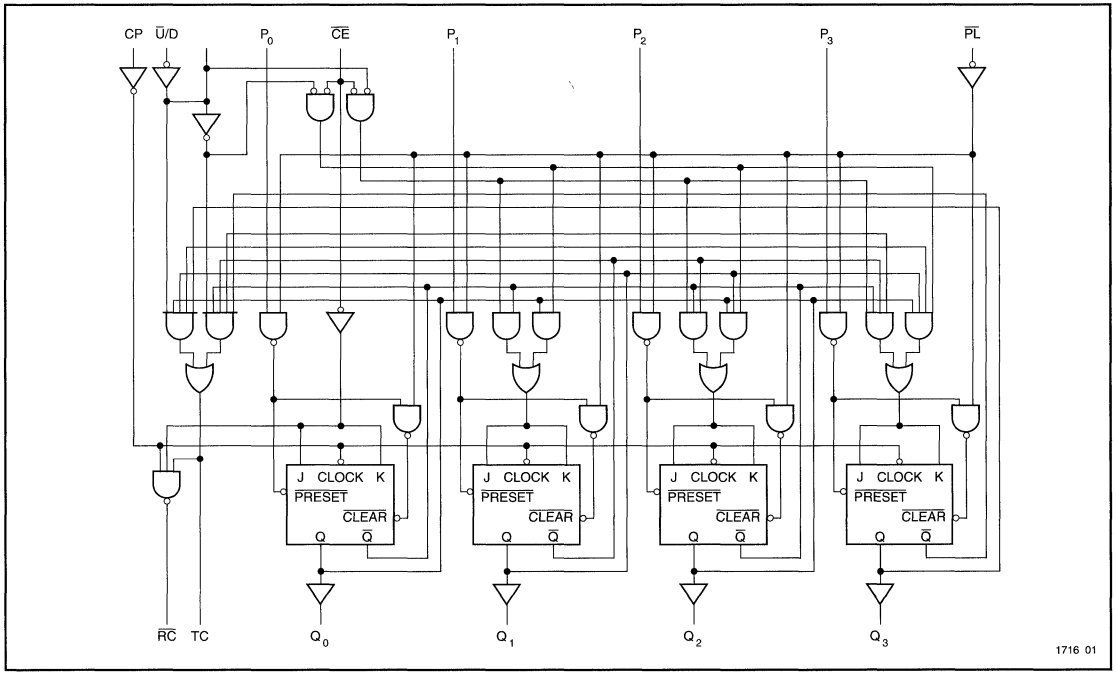
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 6.2ns max. (Com'l) FCT-A speed at 7.8ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**

2

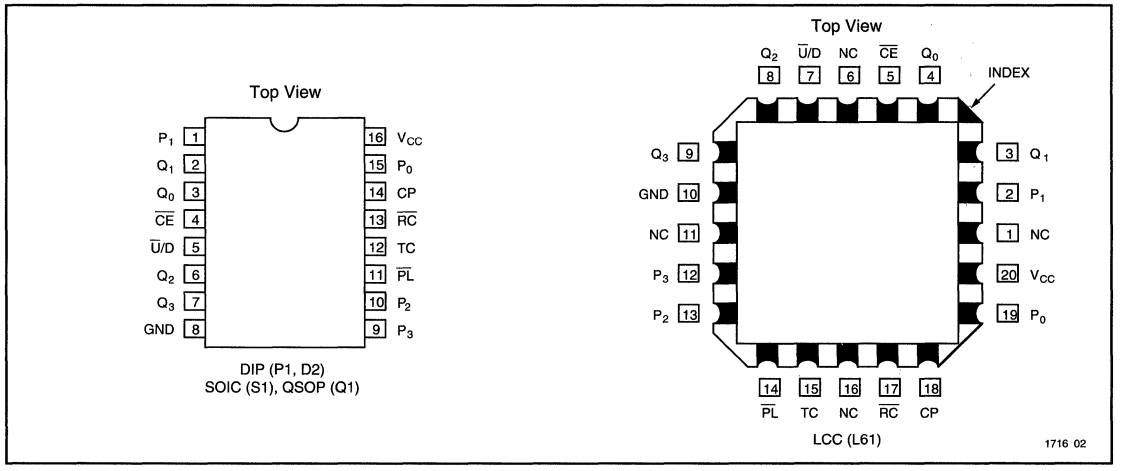
DESCRIPTION

The 'FCT191T is a reversible modulo-16 binary counter, featuring synchronous counting and asynchronous presetting. The preset allows the 'FCT191T to be used in programmable dividers. The count enable input, terminal count output and ripple clock output make possible a variety of methods of implementing multiusage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DEFINITION OF FUNCTIONAL TERMS

Pin Names	Description
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
P_{0-3}	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input (Active LOW)
$\overline{U}$/D	Up/Down Count Control Input
Q_{0-3}	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output (Active LOW)
TC	Terminal Count Output (Active HIGH)

1716 Tbl 01

$\overline{RC}$ FUNCTION TABLE[2]

Inputs		Outputs	
$\overline{CE}$	CP	TC[1]	$\overline{RC}$
L	⊓	H	⊓
H	X	X	H
X	X	L	H

1716 Tbl 02

MODE SELECT FUNCTION TABLE[2]

Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asynchronous)
H	H	X	X	No Change (Hold)

1716 Tbl 03

Notes:

1. TC is generated internally.
2. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care, ⌐ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1716 Tbl 04

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1716 Tbl 05

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1716 Tbl 06

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1716 Tbl 07

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1716 Tbl 08

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, Preset Mode, 50% Duty Cycle, Outputs Open, $\overline{MR}$ = V_{CC} = $\overline{SR}$, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.0	2.8	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = V_{CC}, V_{IN} = GND
		1.2	3.8	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = 3.4V, V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = V_{CC}, V_{IN} = GND,
		4.2	10.5[4]	mA	V_{CC} = MAX, Preset Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 5MHz, $\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND, V_{IN} = 3.4V or V_{IN} =GND

1716 Tbl 09

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

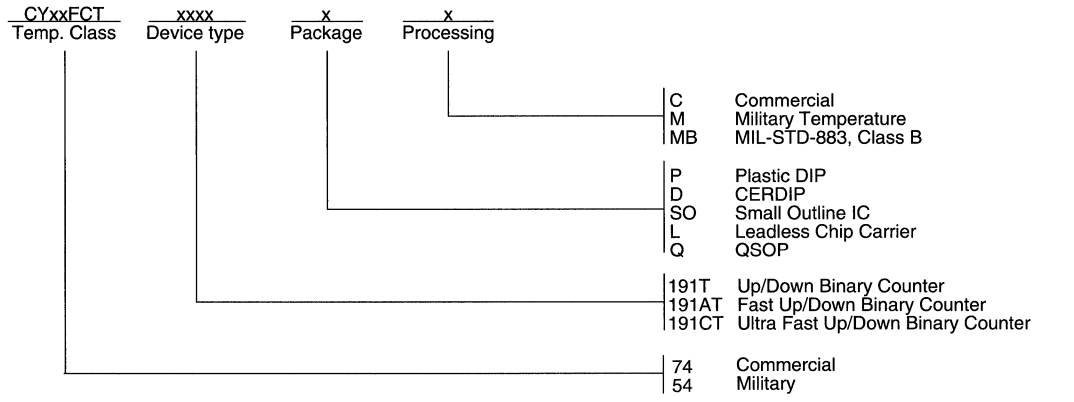
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Condition[1]	'FCT191T				'FCT191AT				'FCT191CT				Units
			MIL		COM'L		MIL		COM'L		MIL		COM'L		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n	C_L = 50pF R_L = 500Ω	1.5	16.0	2.5	12.0	1.5	10.5	2.5	7.8	1.5	8.4	1.5	6.2	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		2.0	16.0	3.0	14.0	2.0	12.2	3.0	11.8	1.5	9.8	1.5	9.4	ns
t_{PLH} t_{PHL}	Propagation Delay CP to $\overline{RC}$		1.5	12.5	2.5	8.5	1.5	10.0	2.5	8.5	1.5	7.9	1.5	6.8	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$		2.0	8.5	2.0	8.0	2.0	8.0	2.0	7.2	1.5	6.4	1.5	6.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$		4.0	22.5	4.0	20.0	4.0	14.7	4.0	13.0	2.5	11.7	2.5	11.0	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{U}$/D to TC		3.0	13.0	3.0	11.0	3.0	8.5	3.0	7.2	1.5	6.8	1.5	6.1	ns
t_{PLH} t_{PHL}	Propagation Delay P_n to Q_n		1.5	16.0	2.0	14.0	1.5	10.4	2.0	9.1	1.5	8.3	1.5	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n		3.0	14.0	3.0	13.0	3.0	9.1	3.0	8.5	2.0	7.3	2.0	7.2	ns
t_{SU}	Set-up Time, HIGH or LOW P_n to $\overline{PL}$		6.0		5.0		5.0		4.0		4.0		3.5		
t_H	Hold Time, HIGH or LOW P_n to $\overline{PL}$		1.5		1.5		1.5		1.5		1.5		1.0		ns
t_{SU}	Set-up Time LOW $\overline{CE}$ to CP		10.5		10.0		9.5		9.0		7.6		7.2		ns
t_H	Hold Time LOW $\overline{CE}$ to CP		0		0		0		0		0		0		ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{U}$/D to CP		12.0		12.0		10.0		10.0		8.5		8.0		ns
t_H	Hold Time, HIGH or LOW $\overline{U}$/D to CP		0		0		0		0		0		0		ns
t_W	$\overline{PL}$ Pulse Width LOW		8.5		6.0		8.0		5.5		6.0		5.0		ns
t_W	Clock Pulse Width HIGH or LOW		7.0		5.0		6.0		4.0[3]		5.0		4.0[3]		ns
t_{REM}	Recovery Time $\overline{PL}$ to CP		7.5		6.0		6.5		5.0		5.0		4.5		ns

1716 Tbl 10

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

ORDERING INFORMATION



1716 03

CY54/74FCT240T
CY54/74FCT244T
8-BIT BUFFERS/LINE DRIVERS

FEATURES

- **Function, pinout and drive compatible with the FCT and F logic**
- **FCT-C speed at 4.1ns max. (Com'l) 'FCT244T FCT-A speed at 4.8ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **64mA Sink Current (Com'l), 48mA (Mil) 15mA Source Current (Com'l), 12mA (Mil)**

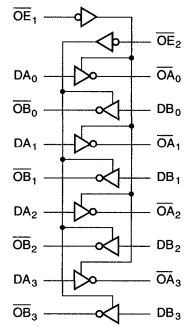
2

DESCRIPTION

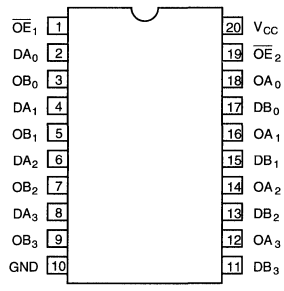
The 'FCT240T and 'FCT244T are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/ receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without external components.

FUNCTIONAL BLOCK DIAGRAM and PIN CONFIGURATIONS

'FCT240T

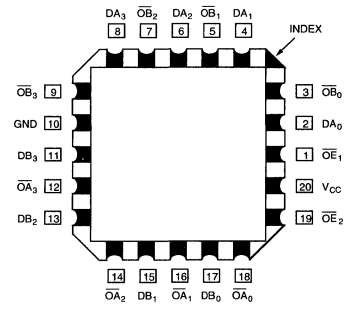


Top View



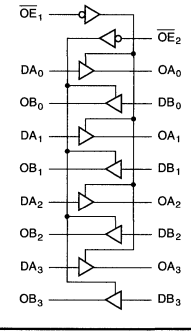
DIP (P5, D6), SOIC (S5), QSOP (Q5)

Top View

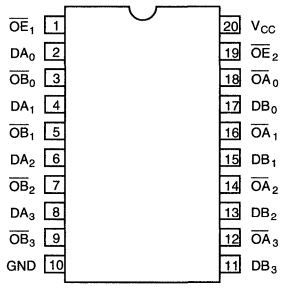


LCC (L61)

'FCT244T

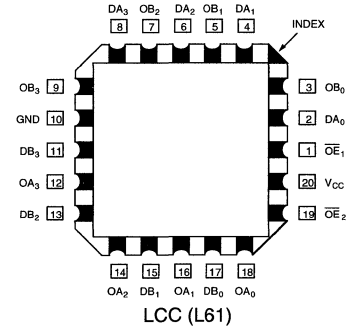


Top View



DIP (P5, D6), SOIC (S5), QSOP (Q5)

Top View



LCC (L61)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			-0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLES

'FCT240T			
Inputs			Output
$\overline{OE}_1$	$\overline{OE}_2$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

'FCT244T			
Inputs			Output
$\overline{OE}_1$	$\overline{OE}_2$	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High Impedance

AC CHARACTERISTICS

Symbol	Parameter	'FCT240T				'FCT240AT				'FCT240CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	1.5	4.7	1.5	4.3	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	1.5	5.7	1.5	5.0	ns	1 7 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	1.5	4.6	1.5	4.5	ns	

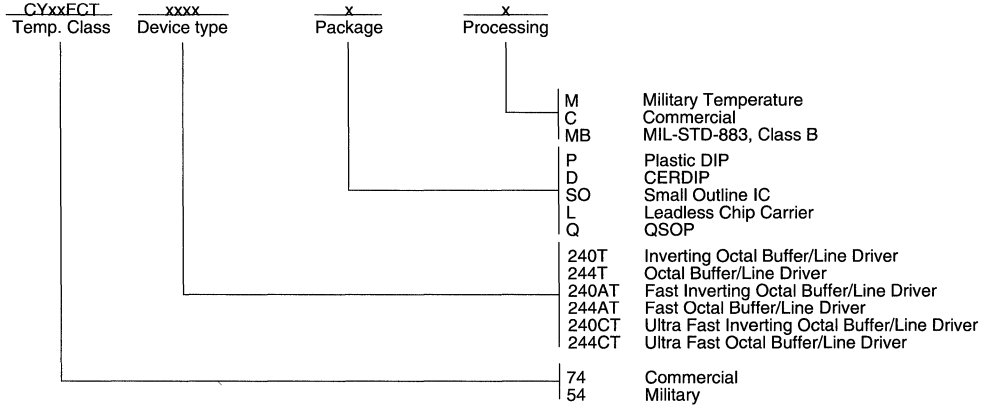
Notes:
* See "Parameter Measurement Information" in the General Information Section.

AC CHARACTERISTICS

Symbol	Parameter	'FCT244T				'FCT244AT				'FCT244CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.8	1.5	4.6	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	1.5	6.5	1.5	5.8	ns	1 7 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	1.5	5.7	1.5	5.2	ns	

Notes:
10. Minimum limits are not guaranteed but are tested on propagation delays.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



FEATURES

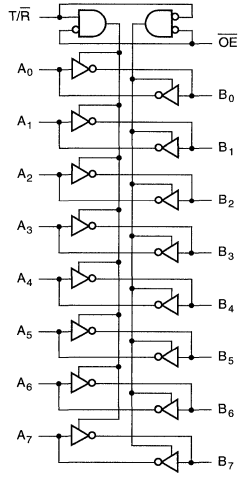
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.1 ns max. (Com'l) FCT-A speed at 4.6 ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**

DESCRIPTION

The 'FCT245T contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus oriented applications. For the 'FC245T, current sinking capability is 64 mA at the A & B ports.

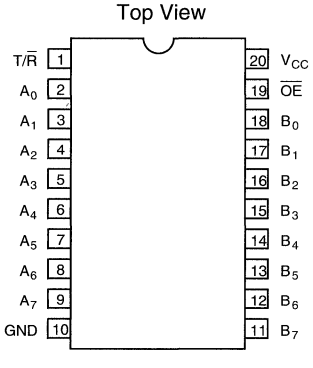
The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable ($\overline{OE}$), when HIGH, disables both the A and B ports by putting them in a high Z condition.

LOGIC BLOCK DIAGRAM

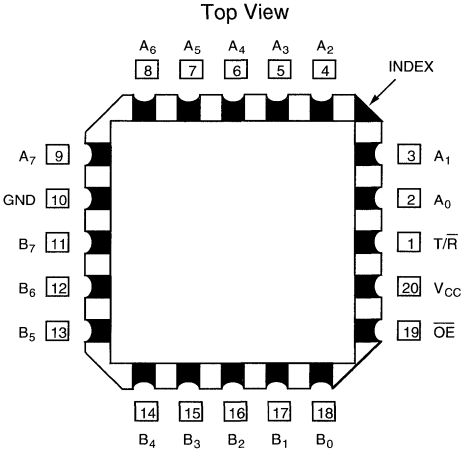


PIN CONFIGURATIONS

'FCT245T



DIP (P5, D6), SOIC (S5), QSOP (Q5)



LCC (61)

1726 01

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1514 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1514 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min.	Max.
Military	–55°C	+125°C
Commercial	0°C	+70°C

1514 Tbl 03

Supply Voltage (V_{CC})	Min.	Max.
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1514 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5Y
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1514 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V,
I_C	Total Power Supply Current[5]	2.0	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.3	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
		3.5	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.5	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

1514 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLES

'FCT245T		
Enable $\overline{OE}$	**Direction Control T/$\overline{R}$**	**Operation**
L	L	$\overline{B}$ Data to Bus A
L	H	$\overline{A}$ Data to Bus B
H	X	High Z State

1514 Tbl 07

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

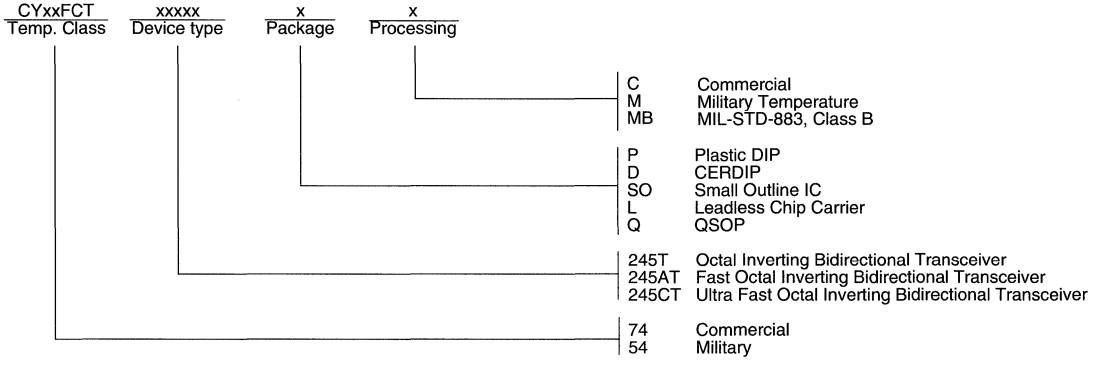
AC CHARACTERISTICS

Symbol	Parameter	'FCT245T				'FCT245AT				'FCT245CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	1.5	4.5	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ or T/$\overline{R}$ to A or B	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	5.2	1.5	4.8	ns	1, 7, 8

1514 Tbl 09

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1726 03

CY54/74FCT257T
QUAD 2-INPUT MULTIPLEXERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.3ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**

DESCRIPTION

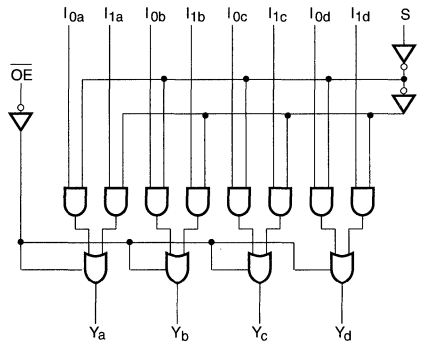
The 'FCT257T has four identical 2-input multiplexers with 3-state outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the select input is HIGH. Data appears at the output in true noninverted form for the 'FCT257T.

The 'FCT257T is a logic implementation of a 4-pole, 2 position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the High-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

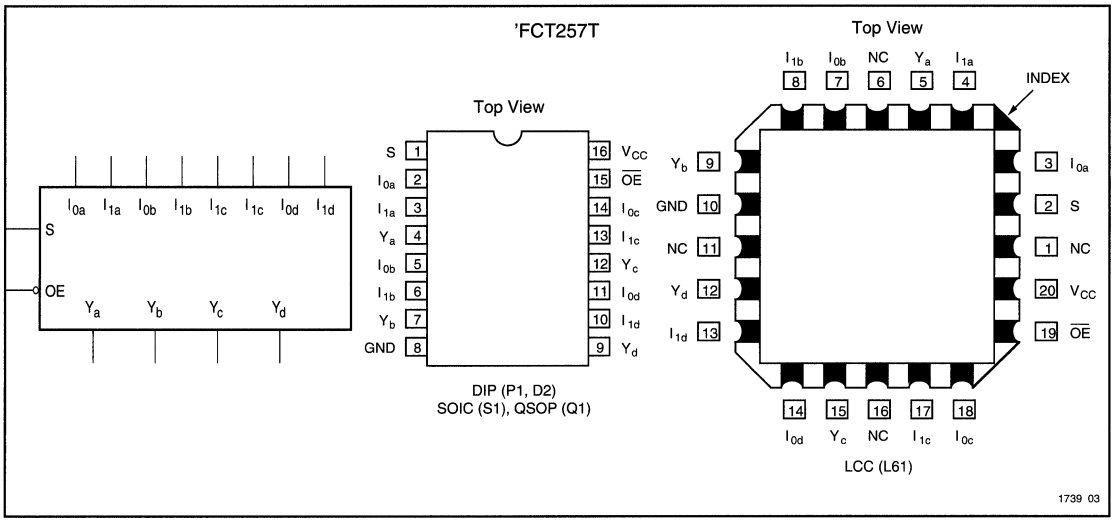
FUNCTIONAL BLOCK DIAGRAM

'FCT257T



1739 01

LOGIC DIAGRAM AND PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1739 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1739 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1739 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1739 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1739 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		1.7	4.0[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.7	8.0[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1739 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE

Inputs				Output
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

1739 Tbl 07

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance (OFF) state

DEFINITION OF FUNCTIONAL TERMS

Pins	Description
$I_{0n} - I_{1n}$	Data inputs
S	Common select input
$\overline{OE}$	Enable input (Active-Low)
$Y_a - Y_d$	Data outputs 'FCT257T

1739 Tbl 08

AC CHARACTERISTICS

Sym.	Parameter	'FCT257T				'FCT257AT				'FCT257CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Prop Delay I_{na}, I_{nb} to Y_n	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay S to O_n	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	1.5	6.0	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time to High or Low	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	1.5	6.8	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time from High or Low	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	1.5	5.3	1.5	5.0	ns	1, 7, 8

1739 Tbl 09

Notes:

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION

CYxxFCT — Temp. Class
xxxxx — Device type
x — Package
x — Processing

Processing	
C	Commercial
M	Military Temperature
MB	MIL-STD-883, Class B
Package	
P	Plastic DIP
D	CERDIP
SO	Small Outline IC
L	Leadless Chip Carrier
Q	QSOP
Device type	
257T	Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
257AT	Fast Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
257CT	Ultra Fast Quad 2-line to 1-line Data Selector/Multiplexer (Non-Inverting)
Temp. Class	
74	Commercial
54	Military

1739 05

CY54/74FCT273T
8-BIT REGISTER

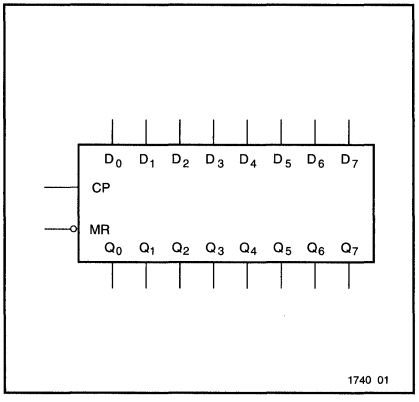
FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.8ns max. (Com'l) FCT-A speed at 7.2ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output**
- **Logic Levels**
  64 mA Sink Current (Com'l), 32 mA (Mil)
- **15 mA Source Current (Com'l), 12 mA (Mil)**
  CMOS for Low-Power Consumption — Typically
- **1/3 of FAST Bipolar Logic**
  Edge Triggered D Flip-Flops
- **Buffered Common Clock**
- **Buffered, Asynchronous Master Reset**
- **Input Clamp Diode to Limit Bus Reflections**

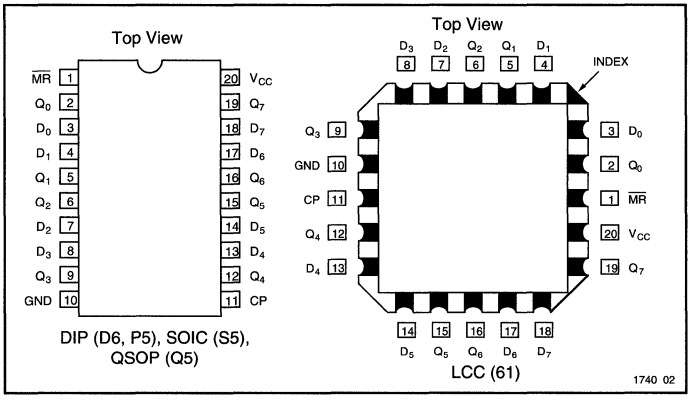
DESCRIPTION

The 'FCT273T consists of eight edge triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered clock (CP) and master reset ($\overline{MR}$) load and reset (clear) all flip-flops simultaneously. The 'FCT273T is an edge triggered register. The state of each D input (one setup time before the low-to-high clock transition) is transferred to the corresponding flip-flop's Q output. All outputs will be forced low by a low voltage level on the $\overline{MR}$ input.

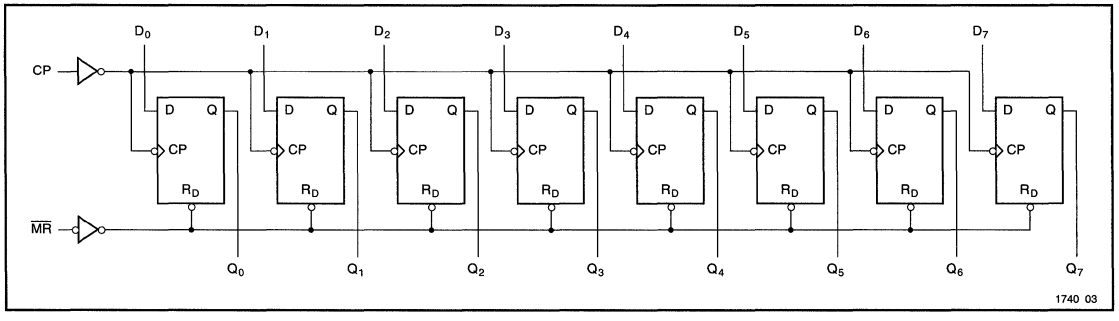
LOGIC SYMBOL



PIN CONFIGURATIONS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1740 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1740 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

2

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1740 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1740 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1740 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{MR}$ = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{MR}$ = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{MR}$ = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{MR}$ = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{MR}$ = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

1740 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs			Output
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load '1'	H	⌐	h	H
Load '0'	H	⌐	l	L

1740 Tbl 07

H = HIGH Voltage Level steady state
h = HIGH Voltage Level one setup time prior to LOW-to-HIGH clock transition
L = LOW Voltage Level steady state
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH transistion
X = Don't Care
⌐ = LOW-to-HIGH clock transition

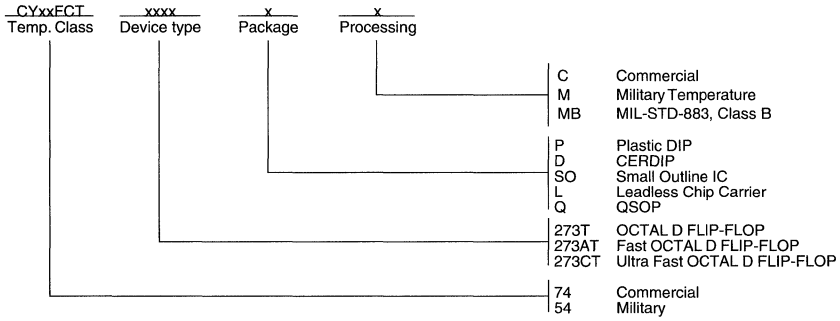
AC CHARACTERISTICS

Symbol	Parameter	'FCT273T				'FCT273AT				'FCT273CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	2.0	6.5	2.0	5.8	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{MR}$ to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	2.0	6.8	2.0	6.1	ns	1, 6
t_s	Set-up Time HIGH or LOW D_n to Clock	3.5	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
t_h	Hold Time HIGH or LOW D_n to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
t_w	Clock Pulse Width HIGH or LOW	7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	5
t_w	$\overline{MR}$ Pulse Width LOW	7.0	—	7.0	—	6.0	—	6.0	—	6.0	—	6.0	—	ns	6
t_{rec}	Recovery Time $\overline{MR}$ to Clock	5.0	—	4.0	—	2.5	—	2.0	—	2.5	—	2.0	—	ns	6

1740 Tbl 08

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1740 04

CY54/74FCT373T
CY54/74FCT573T
8-BIT LATCHES

FEATURES

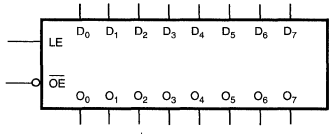
- **Function, Pinout and Drive Compatible with the Fastest Bipolar Logic**
- **FCT-C speed at 4.2ns max. (Com'l) FCT-A speed at 5.2ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.0V) versions of Equivalent and FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

DESCRIPTION

The 'FCT373T and 'FCT573T consist of eight latches with 3-state outputs for bus organized system applications. When latch enable (LE) is high, the flip flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data may be entered into the latches. The 'FCT573T is identical to 'FCT373T except that all the inputs are on one side of the package and the outputs on the other side.

LOGIC SYMBOL

'FCT373T - FCT573T

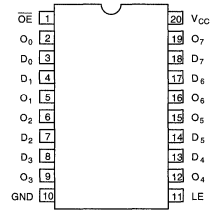


1729 01

PIN CONFIGURATIONS

'FCT373T

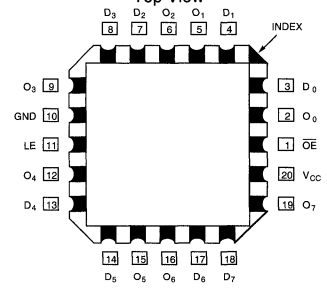
Top View



DIP(D6, P5),SOIC(S5)
QSOP (Q5)

'FCT373T

Top View

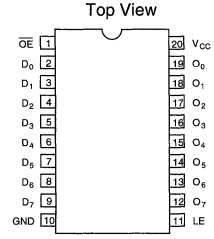


LCC(L61)

1729 02

'FCT573T

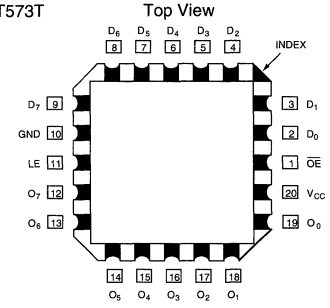
Top View



DIP(D6, P5),SOIC(S5),
QSOP (Q5)

'FCT573T

Top View

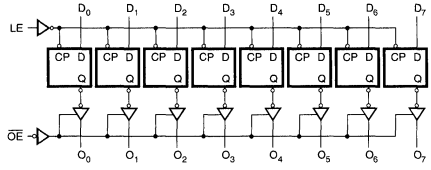


LCC(L61)

1729 03

LOGIC DIAGRAM

'FCT373T - 'FCT573T



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1729 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1729 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

1729 Tbl 03

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C
Supply Voltage (V_{CC})	**Min**	**Max**
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1729 Tbl 04

FUNCTION TABLES (Each Latch)

Inputs			Outputs 'FCT373/'FCT573
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

1729 Tbl 05

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
Q_0 = previous state of flip flops ($\overline{Q}_{n-1}$)
$\overline{Q}_0$ = previous state of flip flops ($\overline{Q}_{n-1}$)

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC} V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC} V_{IN} = 3.4V or V_{IN} = GND

1729 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS ('FCT373T — 'FCT573T)

Sym.	Parameter	'FCT373T 'FCT573T				'FCT373AT 'FCT573AT				'FCT373CT 'FCT573CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Prop Delay D_n to O_n	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	1.5	5.1	1.5	4.2	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay LE to O_n	2.0	15.0	2.0	13.0	2.0	9.8	2.0	8.5	2.0	8.0	2.0	5.5	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	13.5	1.5	12.0	1.5	7.5	1.5	6.5	1.5	6.3	1.5	5.5	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	7.5	1.5	6.5	1.5	5.5	1.5	5.9	1.5	5.0	ns	
$t_s(H)$ $t_s(L)$	Setup Time, High to Low D_n to LE	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	ns	9
$t_n(H)$ $t_n(L)$	Hold Time, High to Low D_n to LE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	
$t_w(H)$	LE Pulse Width High	6.0	–	6.0	–	6.0	–	5.0	–	6.0	–	5.0	–	ns	5

1729 Tbl 10

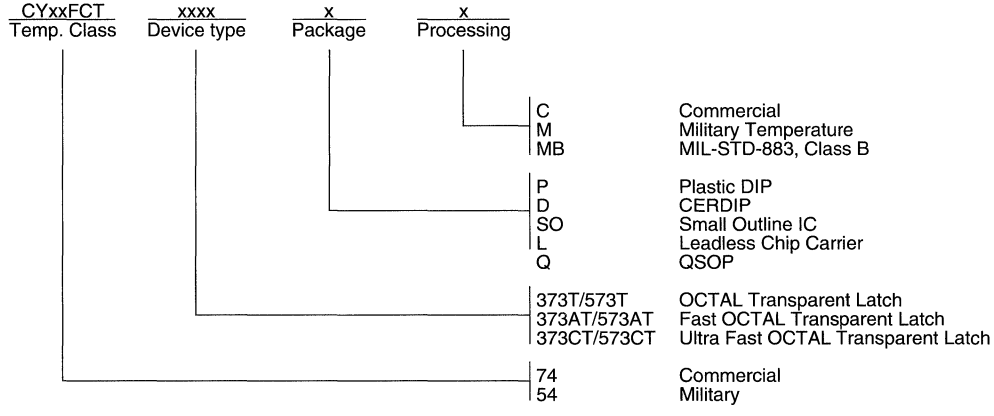
Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.

* AC Characteristics guaranteed with C_L = 50 pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



CY54/74FCT374T
CY54/74 FCT574T
8-BIT REGISTERS

FEATURES

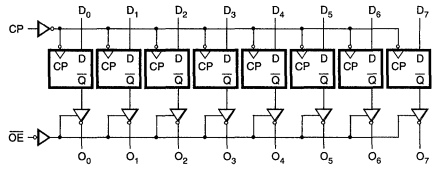
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.2ns max. (Com'l)**
  FCT-A speed at 6.5ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil)**
  15 mA Source Current (Com'l), 12 mA (Mil)
- **Edge Triggered D Type Inputs**
- **250 MHz Typical Toggle Rate**
- **Buffered Positive Edge Triggered Clock**

DESCRIPTION

The 'FCT374T and 'FCT574T are high-speed low power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have 3-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The 'FCT574T is identical to 'FCT374T except that all the outputs are on one side of the package and inputs on the other side. The eight flip-flops contained in the 'FCT374T and 'FCT574T will store the state of their individual D inputs that meet the setup and hold time requirements on the low-to-high clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high impedance state. The state of output enable does not affect the state of the flip-flops.

LOGIC DIAGRAMS

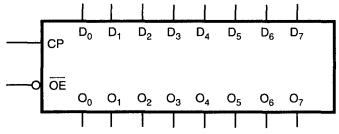
'FCT374T - 'FCT574T



1730 01

LOGIC SYMBOL

'FCT374T -- FCT574T

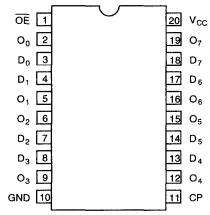


1730 02

PIN CONFIGURATIONS

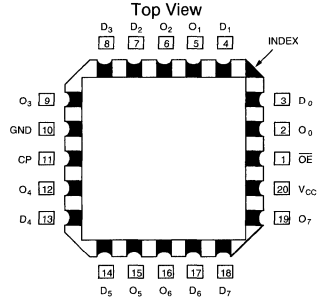
'FCT374T

Top View



DIP(D6, P5), SOIC (S5), QSOP (Q5)

Top View

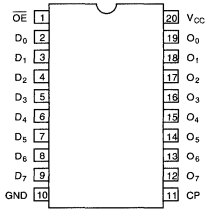


LCC(L61)

1730 03

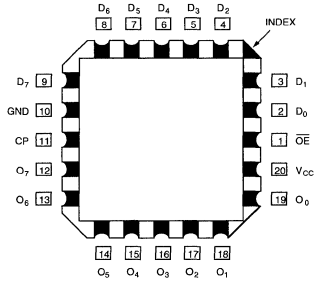
'FCT574T

Top View



DIP(D6, P5), SOIC (S5), QSOP (Q5)

Top View



LCC(L61)

1730 04

2

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1730 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1730 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1730 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1730 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1730 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1730 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs			Outputs 'FCT374T–'FCT574T
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH clock transition
Z = HIGH Impedance

1730 Tbl 07

AC CHARACTERISTICS

Sym.	Parameter	'FCT374T/ 'FCT574T				'FCT374AT/ 'FCT574AT				'FCT374CT/ 'FCT574CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Prop. Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	2.0	6.2	2.0	5.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	1.5	6.2	1.5	5.5	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	1.5	5.7	1.5	5.0	ns	1,7,8

1730 Tbl 08

Note:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

AC CHARACTERISTICS

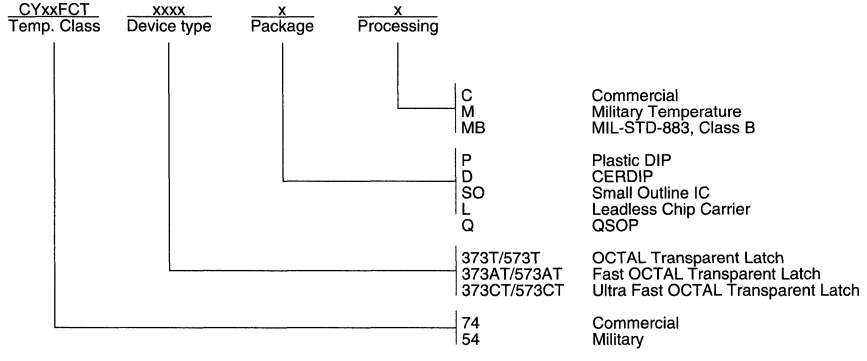
Sym.	Parameter	'FCT374T/ 'FCT574T				'FCT374AT/ 'FCT574AT				'FCT374CT/ 'FCT574CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
$t_S(H)$ $t_S(L)$	Setup Time, High or Low D_n to CP	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	ns	4
$t_n(H)$ $t_n(L)$	Hold Time, High or Low D_n to CP	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	
$t_W(H)$ $t_W(L)$	Clk Pulse Width[2] High or Low	7.0	–	7.0	–	6.0	–	5.0	–	6.0	–	5.0	–	ns	5

1730 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_w(L) = t_w(H) = 4.0ns$ and $t_r = t_f = 1.0ns$.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1730 05

CY54/74FCT377T
8-BIT REGISTER

FEATURES

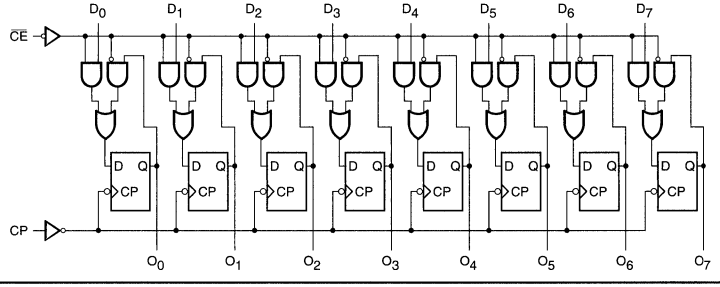
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.2ns max. (Com'l) FCT-A speed at 7.2ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Clock Enable for Address and Data Synchronization Application**
- **Eight Edge-Triggered D Flip-Flops**

2

DESCRIPTION

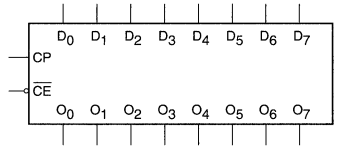
The 'FCT377T have eight edge-triggered, D-type flip-flops with individual D inputs and O outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is LOW. The register is fully edge-triggered. The state of each D input one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

FUNCTIONAL BLOCK DIAGRAM



1735 01

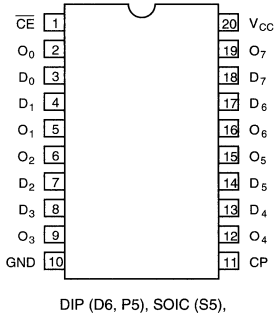
LOGIC SYMBOL



1735 02

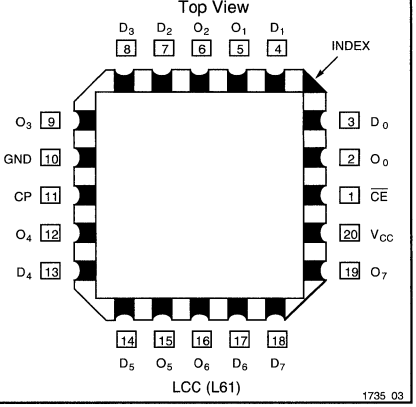
PIN CONFIGURATIONS

Top View



DIP (D6, P5), SOIC (S5), QSOP (Q5)

Top View



LCC (L61)

1735 03

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1735 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1735 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1735 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1735 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$,

1735 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{CE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{CE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{CE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{CE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{CE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1735 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	D	O
Load "1"	⌐¬	l	h	H
Load "0"	⌐¬	l	l	L
Hold (Do Nothing)	⌐¬	h	X	No Change
	X	H	X	No Change

1735 Tbl 07

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
⌐¬ = LOW-to-HIGH Clock Transition

AC CHARACTERISTICS

Symbol	Parameter	'FCT377T				'FCT377AT				'FCT377CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	2.0	15.0	2.0	13.0	2.0	8.3	2.0	7.2	2.0	5.5	2.0	5.2	ns	1, 5

1735 Tbl 08

Note:

1. Minimum limits are guaranteed but not tested on Propagation Delays.

AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT377T				'FCT377AT				'FCT377CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max	Min.[1]	Max.		
t_s(H)	Setup Time, HIGH or LOW Data to CP	3.0	—	2.5	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
t_h(H) t_h(L)	Hold Time, HIGH or LOW Data to CP	2.5	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
t_w(H) t_w(L)	Setup Time, HIGH or LOW $\overline{CE}$ to CP	4.0	—	4.0	—	3.5	—	3.5	—	3.5	—	3.5	—	ns	5
t_w(H) t_w(L)	Hold Time, HIGH or LOW $\overline{CE}$ to CP	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	6
t_w(L)	Clock Pulse Width LOW[2]	7.0	—	7.0	—	7.0	—	6.0	—	7.0	—	6.0	—	ns	6

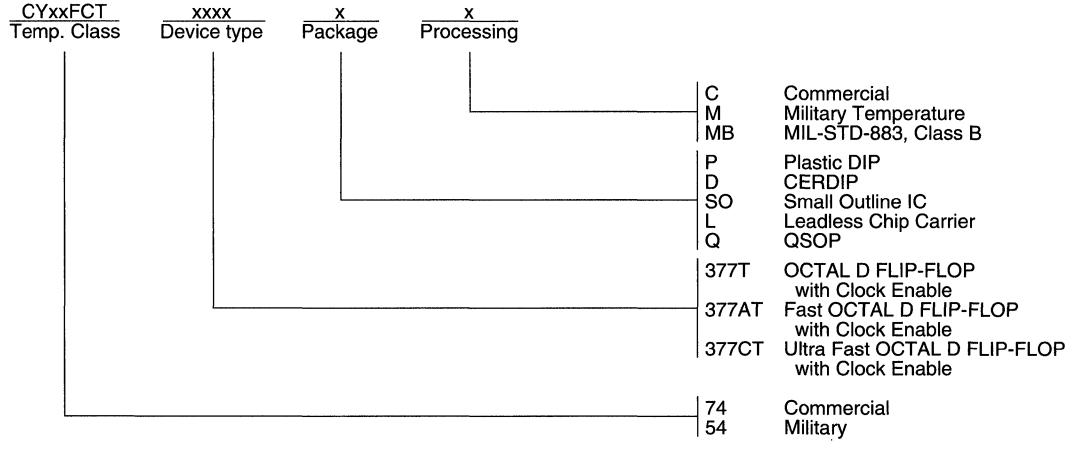
1735 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, t_w(L) = t_w(H) = 4.0ns and t_r = t_f = 1.0ns.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1735 04

CY54/74FCT399T
QUAD 2-INPUT REGISTERS

FEATURES

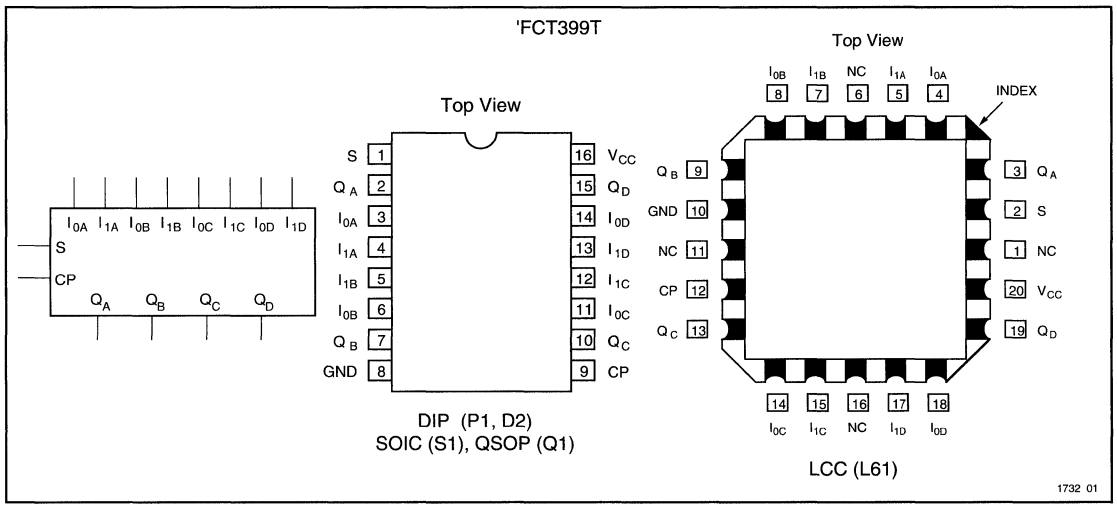
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 6.1ns max. (Com'l) FCT-A speed at 7.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

2

DESCRIPTION

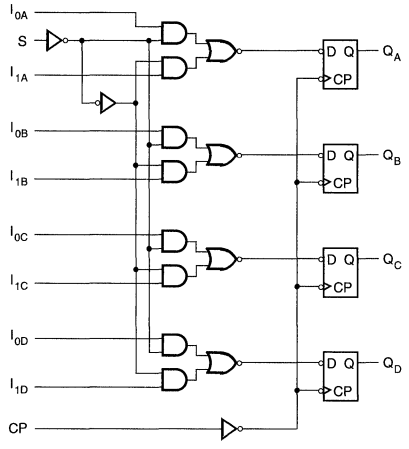
The 'FCT399T is a high-speed quad dual-port registers that select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to- HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0X},I_{1X}) and Select input (S) must be stable only one set-up time prior to, and hold time after, the LOW-to HIGH transition of the Clock input for predictable operation. The 'FCT399T offers true outputs.

LOGIC SYMBOL AND PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM

'FCT399T



1732 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

Notes: 1732 Tbl 01

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C
Supply Voltage (V_{CC})	**Min**	**Max**
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1732 Tbl 02

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

Notes: 1732 Tbl 03

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[1]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, S = Steady State, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 5MHz, S = Steady State, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, 4 Inputs Toggling at f_1 = 5MHz, S = Steady State, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, 4 Inputs Toggling at f_1 = 5MHz, S = Steady State, V_{IN} = 3.4V or V_{IN} = GND

1732 Tbl 04

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLE — 'FCT399T

Inputs			Outputs
S	I_0	I_1	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

1732 Tbl 05

H = HIGH Voltage Level
L = LOW Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Don't Care

PIN DESCRIPTION

Pin Names	Description
S	Common Select Input
CP	Clock Pulse Input (Active Rising Edge)
$I_{0A} - I_{0D}$	Data Inputs from Source 0
$I_{1A} - I_{1D}$	Data Inputs from Source 1
$Q_A - Q_D$	Register True Outputs

1732 Tbl 06

AC CHARACTERISTICS

Symbol	Parameter	'FCT399T				'FCT399AT				'FCT399CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay CP to Q	3.0	11.5	3.0	10.0	2.5	7.5	2.5	7.0	2.5	6.6	2.5	6.1	ns	1, 5

1732 Tbl 07

Note:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See 'Parameter Measurement Information' in the General Information Section.

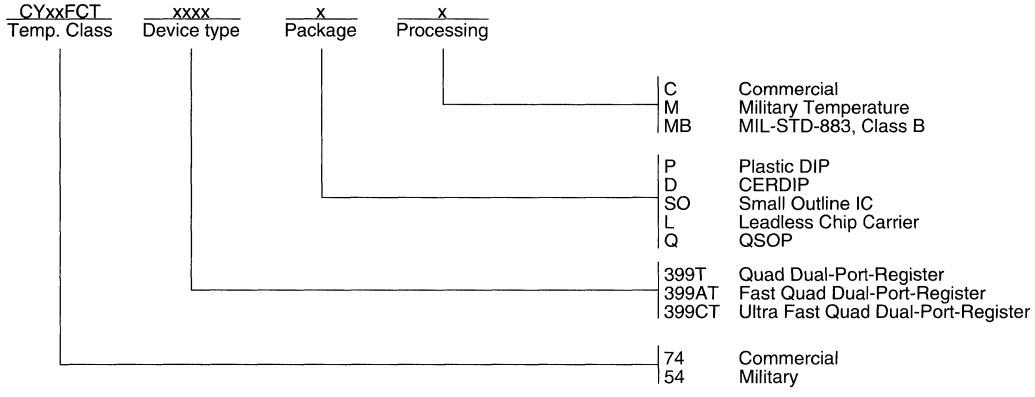
AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT399T				'FCT399AT				'FCT399CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW I_n to CP	4.5	—	4.0	—	4.0	—	3.5	—	4.0	—	3.5	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW I_n to CP	1.5	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns	4
$t_s(H)$ $t_s(L)$	Set-up Time, HIGH or LOW SP to CP	9.5	—	9.0	—	9.0	—	8.5	—	9.0	—	8.5	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW SP to CP	0	—	0	—	0	—	0	—	0	—	0	—	ns	4
$t_w(H)$ $t_w(L)$	Clock Pulse Width[2], HIGH or LOW	7.0	—	5.0	—	6.0	—	5.0	—	6.0	—	5.0	—	ns	5

1732 Tbl 08

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. This parameter is guaranteed but not tested.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1732 03

CY54/74FCT480T
DUAL 8-BIT PARITY GENERATORS/CHECKER

FEATURES

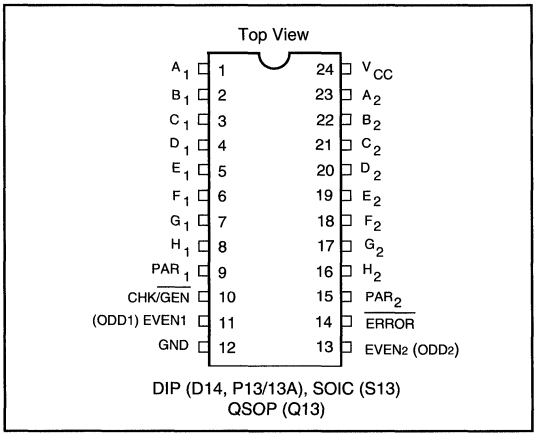
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-A speed at 7.5ns max. (Com'l)**
  FCT-B speed at 5.6ns max. (Com'l)
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil)**
  15 mA Source Current (Com'l), 12 mA (Mil)
- **Two 8-Bit Parity Generator/Checkers Per Device**
- **Open Drain Active Low Parity Error Output**
- **Expandable For Larger Word Widths**

DESCRIPTION

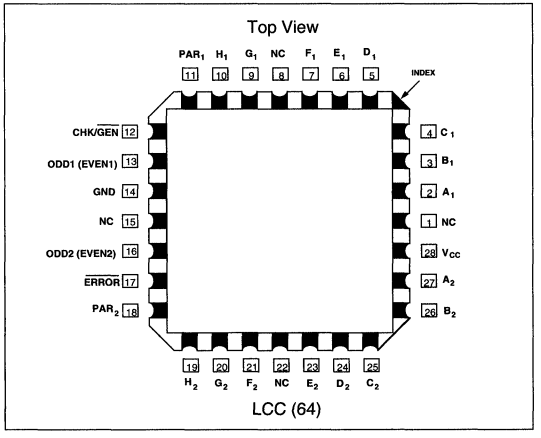
The 'FCT480T is a high speed dual 8-bit parity generator/checkers. Each parity generator/checker accepts eight data bits and one parity bit as inputs, and generates a sum and parity error output. The 'FCT480T can be used in even parity systems.

The parity error output is open-drain, designed for easy expansion of the word width by a wired-OR connection of several 'FCT480T type devices. Since additional logic is not needed, the parity generation or checking times remain the same as for an individual 'FCT480T device.

PIN CONFIGURATIONS



DIP (D14, P13/13A), SOIC (S13)
QSOP (Q13)



LCC (64)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1551 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1551 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS[3]

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1551 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1551 Tbl 04

Notes:

3. Unless otherwise restricted or extended by detail specifications.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1551 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.2	0.35	mA/MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	2.0	5.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.5	7.0	mA	V_{CC} = MAX, Outputs Open, One Bit Toggling at f_1 = 2.5MHz, 50% Duty Cycle, V_{IN} = 3.4V or V_{IN} = GND
		7.25	13.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		10.25	22.75	mA	V_{CC} = MAX, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, 50% Duty Cycle, V_{IN} = 3.4V or V_{IN} = GND

1551 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CCQC} + \Delta I_{CC} \bullet D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS (Minimum values for propagation delays are 1.5 ns, guaranteed by design)

		'FCT480T		'FCT480AT		'FCT480BT		
Symbol	Parameter	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
t_{PLH}	Propagation Delay	17.0	13.0	9.5	7.5	7.0	5.6	ns
t_{PHL}	A_n to EVEN/ODD	16.0	13.0	9.0	7.0	6.6	5.6	ns
t_{PLH}*	Propagation Delay	17.0	13.0	9.0	7.0	7.0	5.6	ns
t_{PHL}	A_n to $\overline{ERROR}$	20.0	16.0	10.5	8.5	8.1	6.5	ns
t_{PLH}	Propagation Delay	15.0	12.0	8.5	6.5	6.3	5.9	ns
t_{PHL}	Chk/$\overline{Gen}$ to EVEN/ODD	18.0	15.0	10.0	7.5	7.4	5.9	ns
t_{PLH}*	Propagation Delay	17.0	14.0	9.5	7.5	7.1	5.7	ns
t_{PHL}	Chk/$\overline{Gen}$ to $\overline{ERROR}$	16.0	13.0	9.0	7.0	6.9	5.5	ns

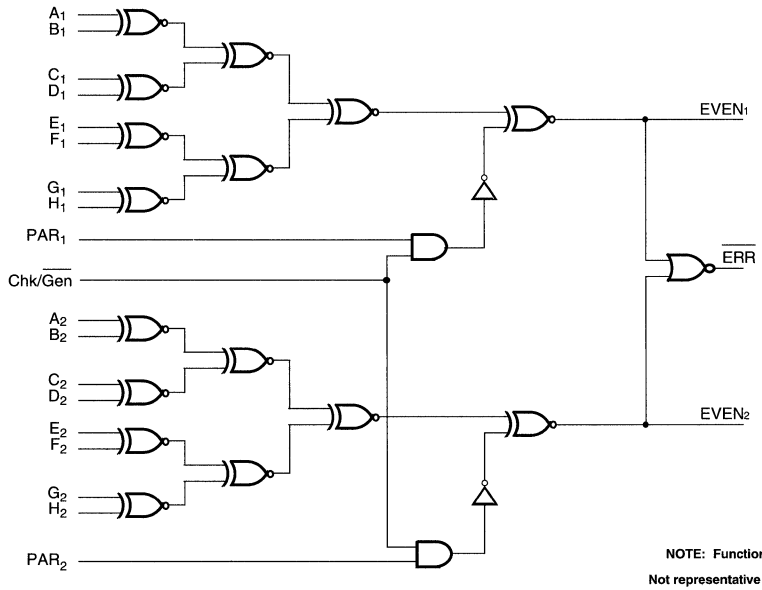
*t_{PLH} is measured up to $V_{OUT} = V_{OL} + 0.3V$

1551 Tbl 07

'FCT480T TRUTH TABLE

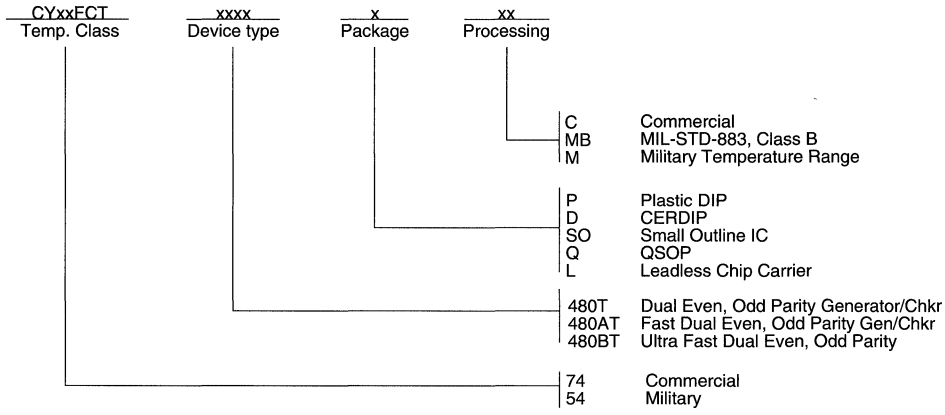
Inputs					Outputs		
A1 to H1	**A2 to H2**	**CHK/$\overline{GEN}$**	**PAR1**	**PAR2**	**EVEN1**	**EVEN2**	**$\overline{ERROR}$**
Number of A1 to H1 Inputs HIGH is EVEN	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	L	L	H
			L	H	H	L	L
			H	L	L	H	L
			L	L	H	H	L
		L	X	X	H	H	L
	Number of Inputs HIGH A2 to H2 is ODD	H	H	H	L	H	L
			L	H	H	H	L
			H	L	L	L	H
			L	L	H	L	L
		L	X	X	H	L	L
Number of A1 to H1 Inputs HIGH is ODD	Number of A2 to H2 Inputs HIGH is EVEN	H	H	H	H	L	L
			L	H	L	L	H
			H	L	H	H	L
			L	L	L	H	L
		L	X	X	L	H	L
	Number of A2 to H2 Inputs HIGH is ODD	H	H	H	H	H	L
			L	H	L	H	L
			H	L	H	L	L
			L	L	L	L	H
		L	X	X	L	L	H

FUNCTIONAL BLOCK DIAGRAM



NOTE: Functional description only.
Not representative of propagation delays.

ORDERING INFORMATION



CY54/74FCT540T
CY54/74FCT541T
8-BIT BUFFERS/LINE DRIVERS

FEATURES

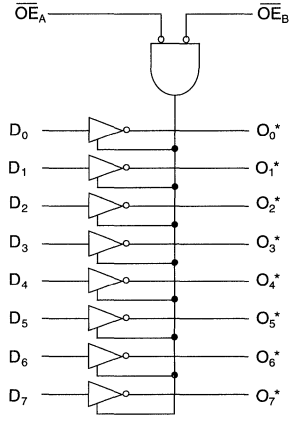
- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 4.3ns max. (Com'l) FCT-A speed at 4.8ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **3-State Outputs**

2

DESCRIPTION

The 'FCT540T and the 'FCT541T are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers. The devices provide speed and drive capabilities equivalent to their fastest bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without external components.

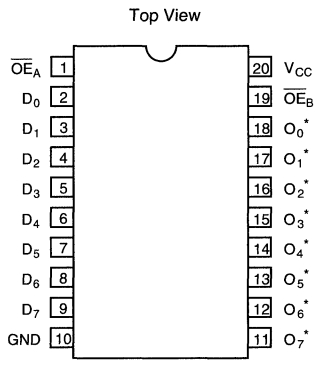
FUNCTIONAL BLOCK DIAGRAM



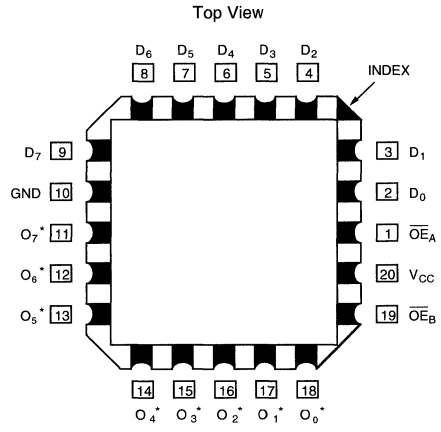
'FCT540T/541T

*$\overline{O}_n$ for 'FCT540T

PIN CONFIGURATIONS



DIP (D6,P5),
SOIC (S5), QSOP (Q5)



LCC (L61)

1742 01

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1742 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1742 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1742 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1742 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1742 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} V_{IN} = 3.4V or V_{IN} = GND

1742 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLES

'FCT540T

Inputs			Output
$\overline{OE}_A$	$\overline{OE}_B$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

1742 Tbl 07

'FCT541T

Inputs			Output
$\overline{OE}_A$	OE_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

1742 Tbl 08

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High Impedance

AC CHARACTERISTICS

Symbol	Parameter	'FCT540T 'FCT541T				'FCT540AT 'FCT541AT				'FCT540CT 'FCT541CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output(540)	1.5	9.5	1.5	8.5	1.5	5.1	1.5	4.8	1.5	4.7	1.5	4.3	ns	1, 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output(541)	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	1.5	4.6	1.5	4.1	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	1.5	6.5	1.5	5.8	ns	1, 7
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	1.5	5.7	1.5	5.2	ns	8

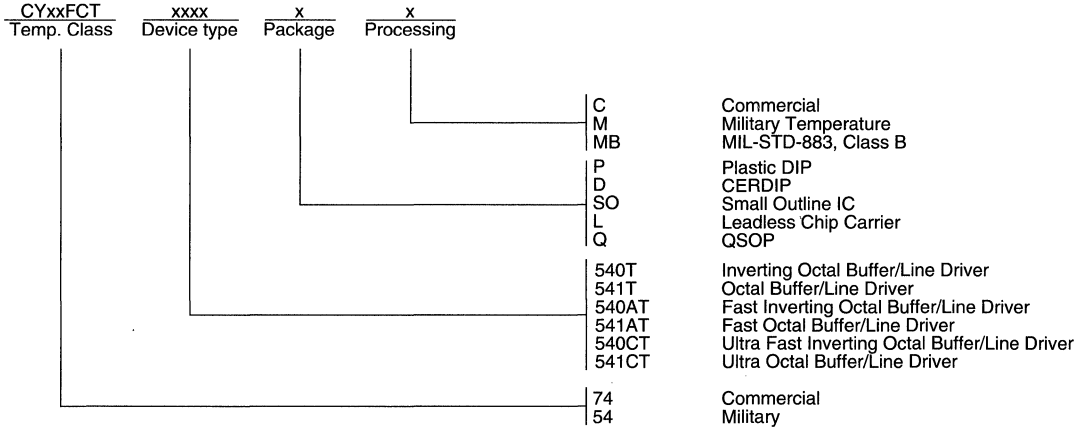
1742 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1742 02

CY54/74FCT543T
8-BIT LATCHED TRANSCEIVER

FEATURES

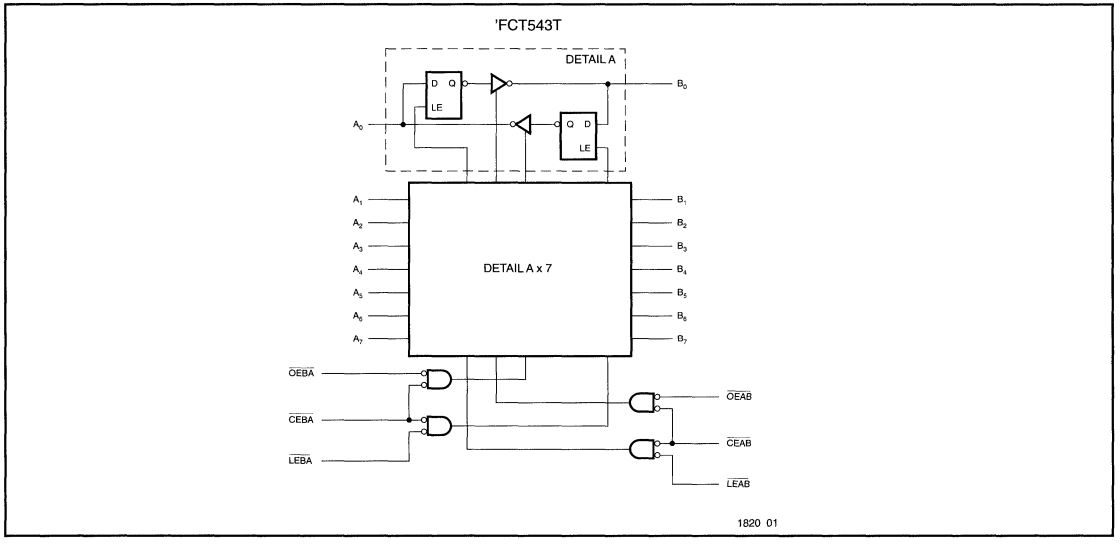
- **Function, Pinout, and Drive Compatible with the FCT and F Logic**
- **FCT-A speed at 5.3ns max. (Com'l) FCT speed at 6.5ns max. (Com'l)**
- **CMOS V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Separate Controls for Data Flow in Each Direction**
- **Back to Back Latches for Storage**

2

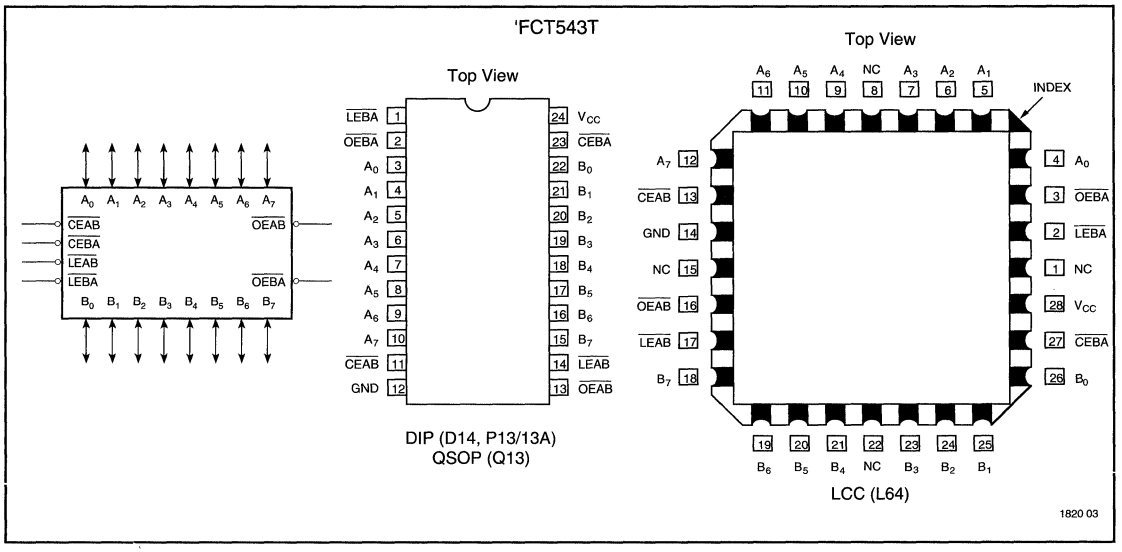
DESCRIPTION

The 'FCT543T T Octal Latched Transceiver contains two sets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latchs in the storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$ and $\overline{OEAB}$ inputs.

FUNCTIONAL BLOCK DIAGRAM



LOGIC SYMBOL AND PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

1820 Tbl 01

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1820 Tbl 02

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to 7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to 7.0	V

1820 Tbl 03

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1820 Tbl 04

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1820 Tbl 05

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage			0.8		V		
V_H	Hysteresis[1]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_{IH}	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current[3]	Except I/O Pin			5	µA	MAX	V_{IN} = 2.7V
		I/O Pin			15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]	Except I/O Pin			–5	µA	MAX	V_{IN} = 0.5V
		I/O Pins only			–15	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				15	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	MAX	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
$C_{I/O}$	Output Capacitance[3]			9	12	pF		All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC}$–0.2V

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

1820 Tbl 06

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[1]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{CEAB}$ + $\overline{OEAB}$ = Low, Outputs Open, $\overline{CEAB}$ = High, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND

1820 Tbl 09

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

Inputs			Latch Status	Outputs 'FCT543T
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0–B7
H	–	–	Storing	High Z
–	H	–	Storing	–
–	–	H	–	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

1820 Tbl 10

* = Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
– = Don't Care or Irrelevent
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$

AC CHARACTERISTICS

Sym.	Parameter	'FCT543T				'FCT543AT				'FCT543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	2.5	6.1	2.5	5.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n $\overline{LEAB}$ to B_n	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	2.5	8.0	2.5	7.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	2.0	9.0	2.0	8.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	2.0	7.5	2.0	6.5	ns	1,7,8

1820 Tbl 11

Notes:
1. Minimum limits are guaranteed on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

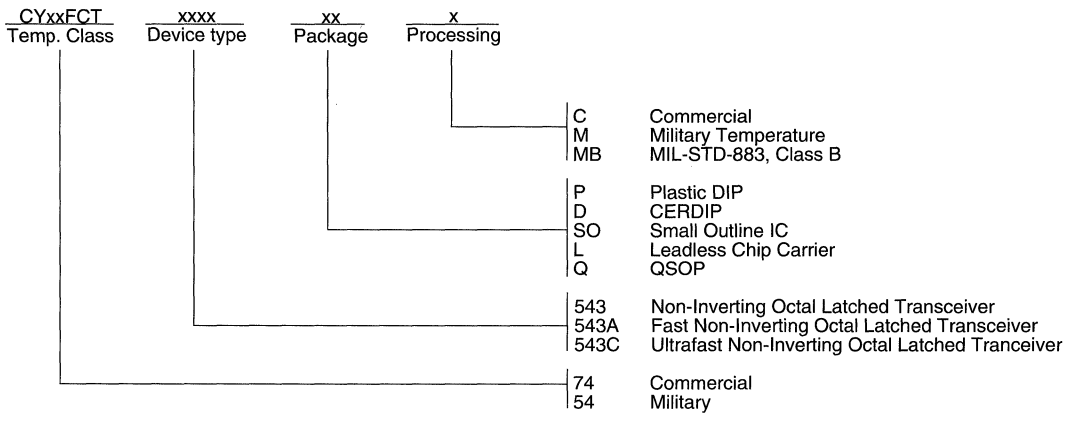
AC OPERATING REQUIREMENTS

Sym.	Parameter	'FCT543T				'FCT543AT				'FCT543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_s (H) t_s (L)	Set-up Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	6

1820 Tbl 12

Note:
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1820 05

CY54/74FCT646T
CY54/74FCT648T
8-BIT REGISTERED TRANSCEIVERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Independent Register for A and B Buses**
- **3-State Output**

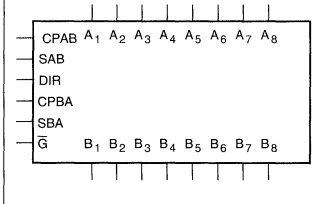
2

DESCRIPTION

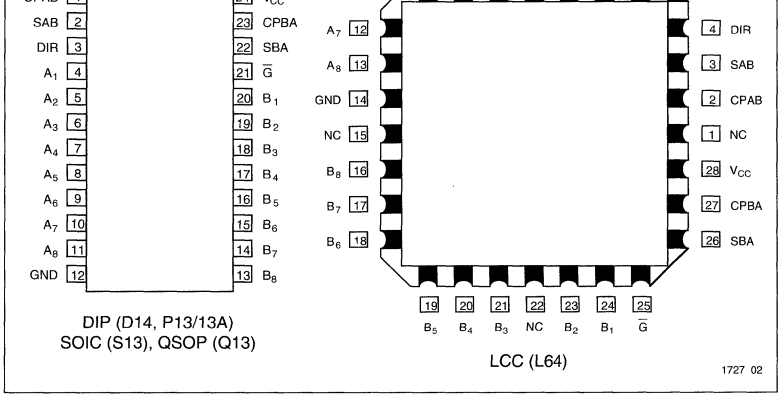
The 'FCT646T and 'FCT648T consist of a bus tranceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function.

In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable control $\overline{G}$ is Active LOW. In the isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

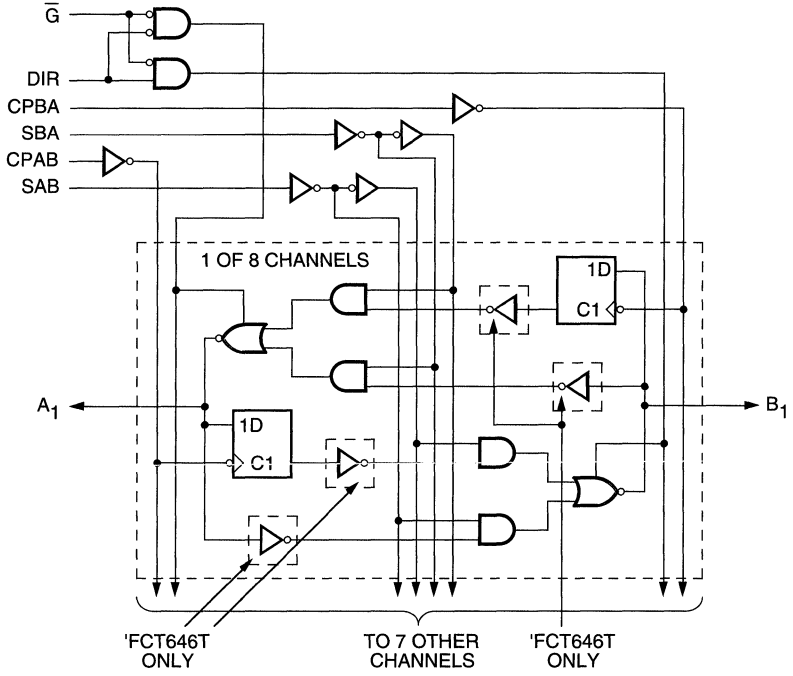
LOGIC SYMBOL



PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM

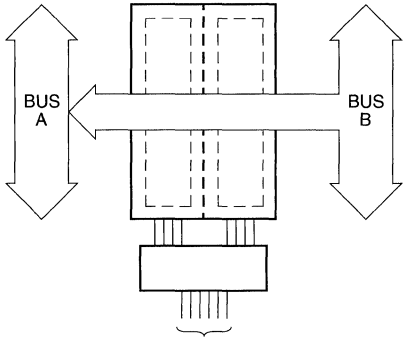


1727 03

PIN DESCRIPTION

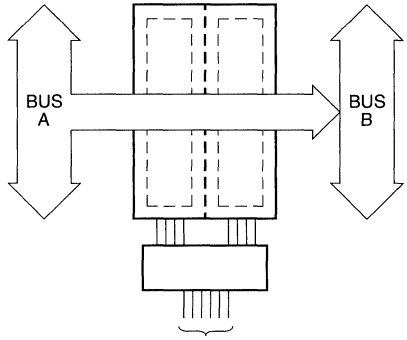
Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

1727 Tbl 01



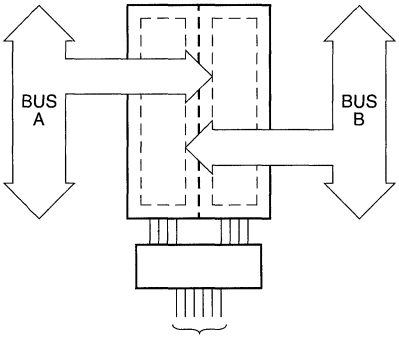
REAL-TIME TRANSFER BUS B TO BUS A

1727 04



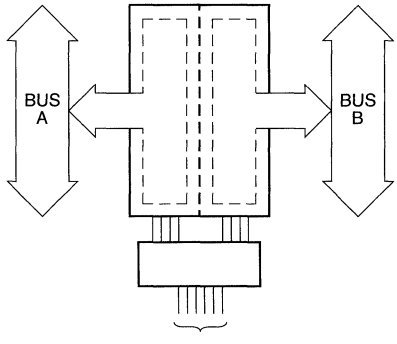
REAL-TIME TRANSFER BUS A TO BUS B

1727 05



STORAGE FROM A AND/OR B

1727 06



TRANSFER STORED DATA TO A AND/OR B

1727 07

Note:
1. Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLE

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT646T	'FCT648T
H H	X X	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

1727 Tbl 02

Notes:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are alwaysenabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↓ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1727 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1727 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1727 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1727 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1727 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1727 Tbl 08

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT646T/648T				'FCT646AT/648AT				'FCT646CT/648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A or B	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

1727 Tbl 09

Notes:

* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.
* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

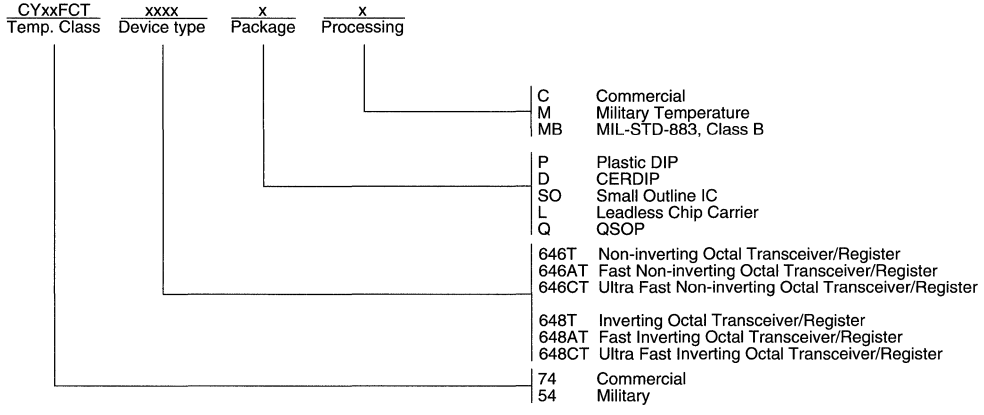
Symbol	Parameter	'FCT646T/648T				'FCT646AT/648AT				'FCT646CT/648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_s(H) t_s(L)	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
t_h(H) t_h(L)	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
t_w(H) t_w(L)	Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	5

1727 Tbl 10

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1727 08

CY54/74FCT652T
8-BIT REGISTERED TRANSCEIVER

FEATURES

- **Function, Pinout and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 48 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Independent Register for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfer**
- **Bidirectional Bus Transceiver and Registers**

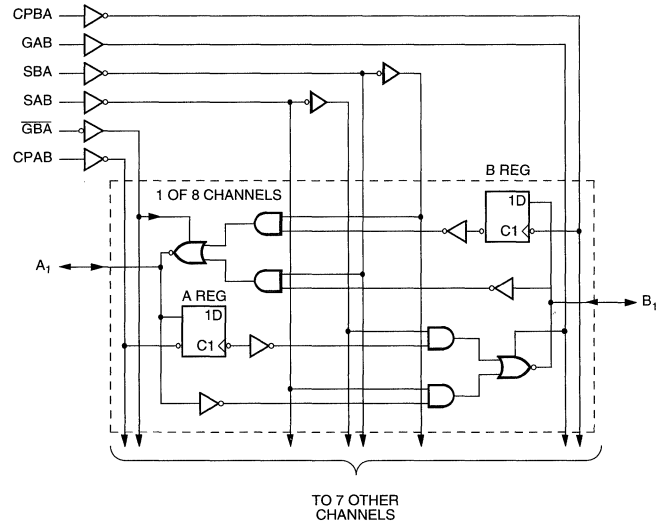
2

DESCRIPTION

THE 'FCT651T consists of bus tranciever circuits, D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

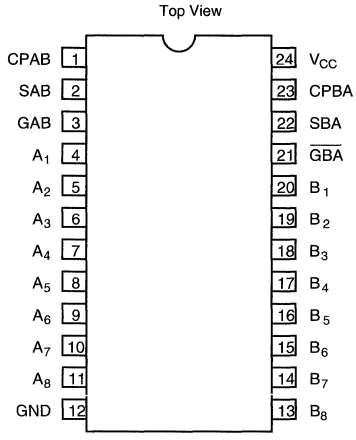
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and $\overline{GBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

FUNCTIONAL BLOCK DIAGRAM

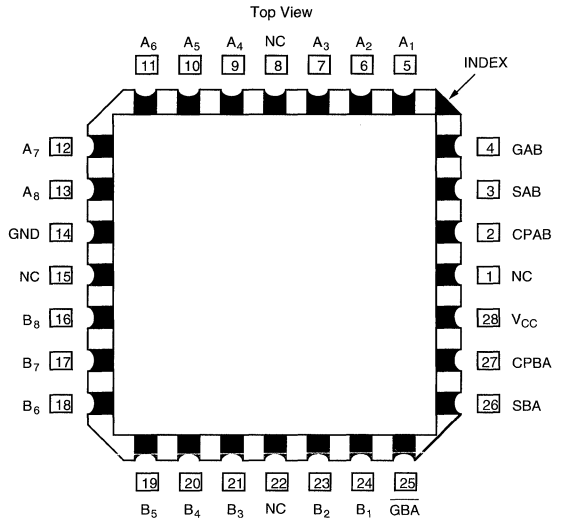


1728 01

PIN CONFIGURATIONS



DIP (D14, P13/13A)
SOIC (S13), QSOP (Q13)



LCC (L64)

1727 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1728 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1728 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1728 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1728 Tbl 04

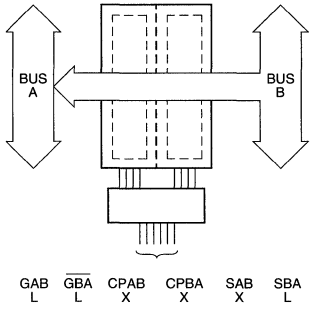
DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1728 Tbl 05

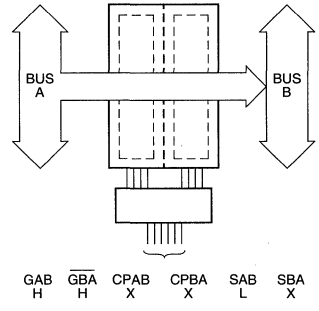
Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.



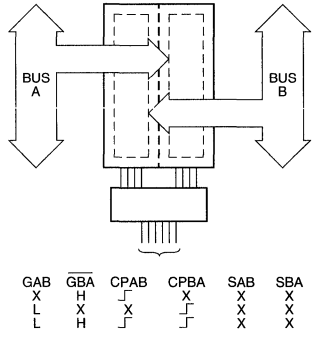
REAL-TIME TRANSFER BUS B TO BUS A

1727 03



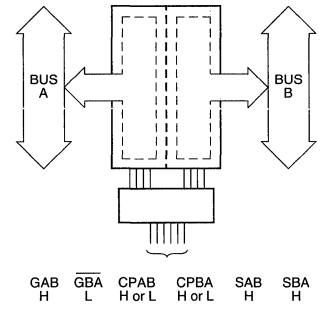
REAL-TIME TRANSFER BUS A TO BUS B

1727 04



STORAGE FROM A AND/OR B

1727 05



TRANSFER STORED DATA TO A AND/OR B

1727 06

Note:

1. Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLES

Inputs						Data I/O		Operation or Function
GAB	**$\overline{GBA}$**	**CPAB**	**CPBA**	**SAB**	**SBA**	**A_1 thru A_8**	**B_1 thru B_8**	**'FCT652T**
L L	H H	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data
X H	H H	↓ ↓	H or L ↓	X X[2]	X X	Input Input	Unspecified[1] Output	Store A, Hold B Store A in both registers
L L	X L	H or L ↓	↓ ↓	X X	X X[2]	Unspecified[1] Output	Input Input	Hold A, Store B Store B in both registers
L L	L L	X X	X H or L	X X	L H	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored $\overline{B}$ Data to A Bus

Notes:

1728 Tbl 06

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ↓ LOW-to-HIGH Transition

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open GAB = GND, $\overline{GBA}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		9.2	21.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

1728 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} \bullet D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT652T				'FCT652AT				'FCT652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 5
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 7, 8

1728 Tbl 08

Notes:

* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

Symbol	Parameter	'FCT652T				'FCT652AT				'FCT652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	1, 4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 4
$t_w(H)$ $t_w(L)$	Clock Pulse Width, HIGH or LOW[2]	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	1, 5

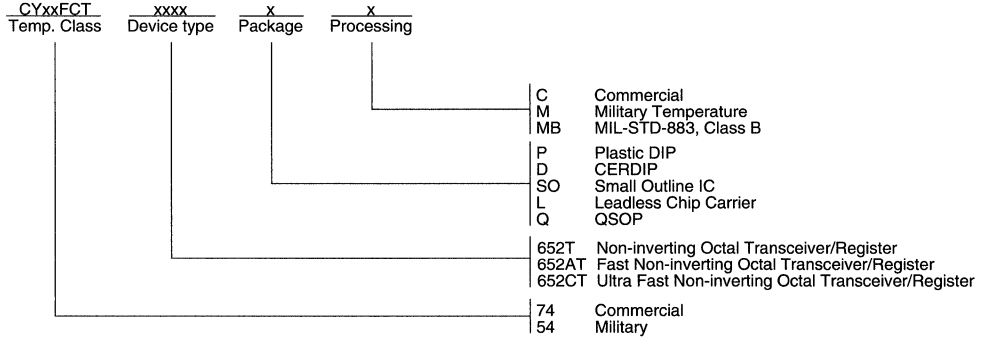
1728 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_w(L) = t_w(H) = 4.0$ns and $t_r = t_f = 1.0$ns.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



CY54/74FCT821T
CY54/74FCT823T
CY54/74FCT825T
8/9/10-BIT BUS INTERFACE REGISTERS

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F and Am29821/23/25 Logic**
- **FCT-C speed at 6.0ns max. (Com'l) FCT-B speed at 7.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **High-Speed Parallel Registers with positive edge-triggered D-type Flip-Flops**
- **Buffered Common Clock Enable ($\overline{EN}$) and Asynchronous Clear Input ($\overline{CLR}$)**

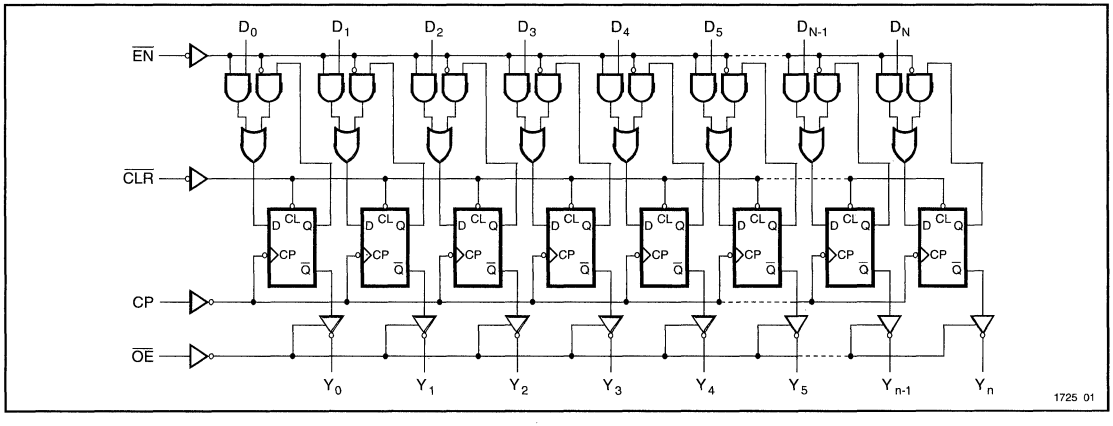
2

DESCRIPTION

The 'FCT820T series bus interface registers are designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/ data paths or buses carrying parity. The 'FCT821T is a buffered, 10 bit wide version of the popular 'FCT374 function. The 'FCT823T is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$) — ideal for parity bus interfacing in high-performance microprogrammed systems. The 'FCT825T is a 8-bit buffered register with all the 'FCT823T controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiuser control of the interface, e.g., $\overline{CS}$, DMA and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The 'FCT800T family of devices are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

FUNCTIONAL BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

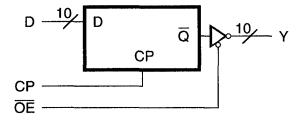
	Device		
Non-inverting	**10-Bit**	**9-Bit**	**8-Bit**
	'FCT821T	'FCT823T	'FCT825T

1725 Tbl 01

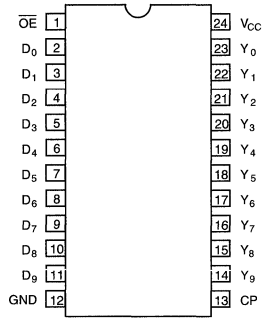
LOGIC SYMBOLS

PIN CONFIGURATONS

'FCT821T (10-Bit Register)

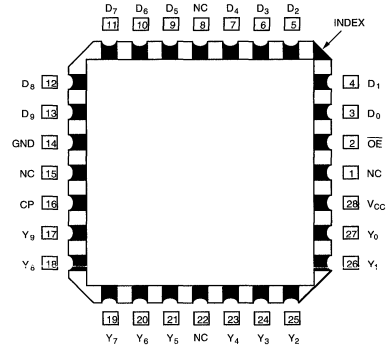


Top View



DIP (D14,P13/13A), SOIC (S13)
QSOP (Q13)

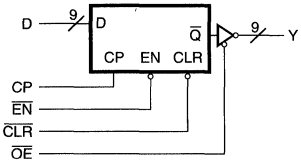
Top View



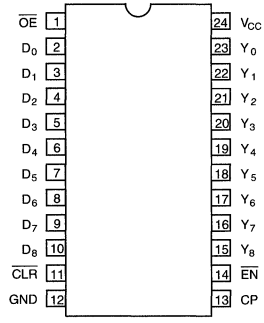
LCC (L64)

1725 02

'FCT823T (9-Bit Register)

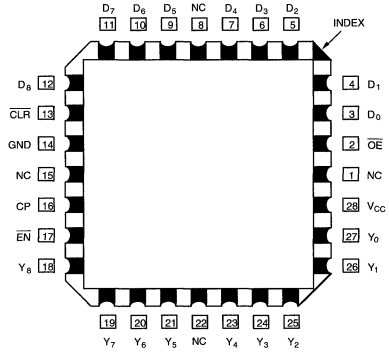


Top View



DIP (D14,P13/13A), SOIC (S13)
QSOP (Q13)

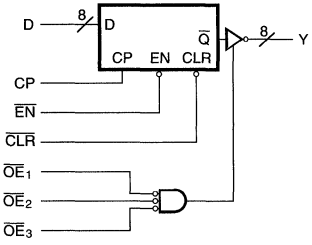
Top View



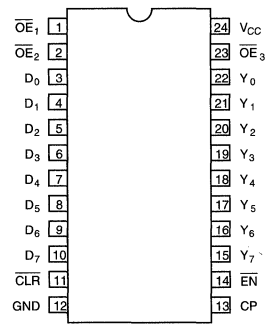
LCC (L64)

1725 03

'FCT825T (8-Bit Register)

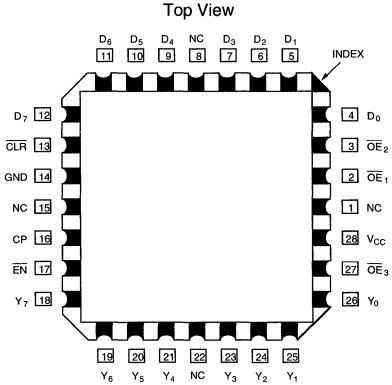


Top View



DIP (D14,P13/13A), SOIC (S13)
QSOP (Q13)

Top View



LCC (L64)

1725 04

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1725 Tbl 02

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1725 Tbl 03

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1725 Tbl 04

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1725 Tbl 05

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1725 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[3]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = $\overline{EN}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = $\overline{EN}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = $\overline{EN}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = $\overline{EN}$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		6.2	16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = $\overline{EN}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1725 Tbl 07

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT821AT–825AT				'FCT821BT–825BT				'FCT821CT–825CT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay CP to Y_1 ($\overline{OE}$ = LOW)	C_L = 50pF R_L = 500Ω	–	11.5	–	10.0	–	8.5	–	7.5	–	7.0	–	6.0	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay CP to Y_1 ($\overline{OE}$ = LOW)	C_L = 300pF[2] R_L = 500Ω	–	20.0	–	20.0	–	16.0	–	15.0	–	13.5	–	12.5	ns	1,5
t_{PLH}	Propagation Delay $\overline{CLR}$ to Y_1	C_L = 50pF R_L = 500Ω	–	15.0	–	14.0	–	9.5	–	9.0	–	8.5	–	8.0	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	–	13.0	–	12.0	–	9.0	–	8.0	–	8.0	–	7.0	ns	1,7,8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 300pF[2] R_L = 500Ω	–	25.0	–	23.0	–	16.0	–	15.0	–	13.5	–	12.5	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 5pF[2] R_L = 500Ω	–	8.0	–	7.0	–	7.0	–	6.5	–	6.2	–	6.2	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	–	9.0	–	8.0	–	8.0	–	7.5	–	6.5	–	6.5	ns	1,7,8

1725 Tbl 08

AC OPERATING REQUIREMENTS

Sym.	Parameter	Test Conditions	'FCT821AT–825AT				'FCT821BT–825BT				'FCT821CT–825CT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{SU}	Data to CP Set-up Time	C_L = 50pF R_L = 500Ω	4.0	–	4.0	–	3.0	–	3.0	–	3.0	–	3.0	–	ns	4
t_h	Data CP Hold Time		2.0	–	2.0	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	4
t_{su}	Enable $\overline{EN}$ to CP Set-up Time		4.0	–	4.0	–	3.0	–	3.0	–	3.0	–	3.0	–	ns	9
t_h	Enable $\overline{EN}$ to CP Hold Time		2.0	–	2.0	–	0.0	–	0.0	–	0.0	–	0.0	–	ns	9
t_{REM}	Clear Recovery Time $\overline{CLR}$ to CP		7.0	–	6.0	–	6.0	–	6.0	–	6.0	–	6.0	–	ns	6
t_w	Clock Pulse Width		7.0	–	7.0	–	6.0	–	6.0	–	6.0		6.0	–	ns	5
t_W	$\overline{CLR}$ Pulse Width LOW		7.0	–	6.0	–	6.0	–	6.0	–	6.0		6.0	–	ns	5

1725 Tbl 09

Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

* See "Parameter Measurement Information" in the General Information Section.

PIN DESCRIPTION

Name	I/O	Description
D_1	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW and $\overline{OE}$ is LOW, the Q_1 outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	O	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
$Y_1, \overline{Y}_1$	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the clock enable is LOW, data on the D_1 input is transferred to the Q_1 output on the LOW-to HIGH clock transition. When the clock enable is HIGH, the Q_1 outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_1 outputs are in the high impedence state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_1 outputs.

1725 Tbl 10

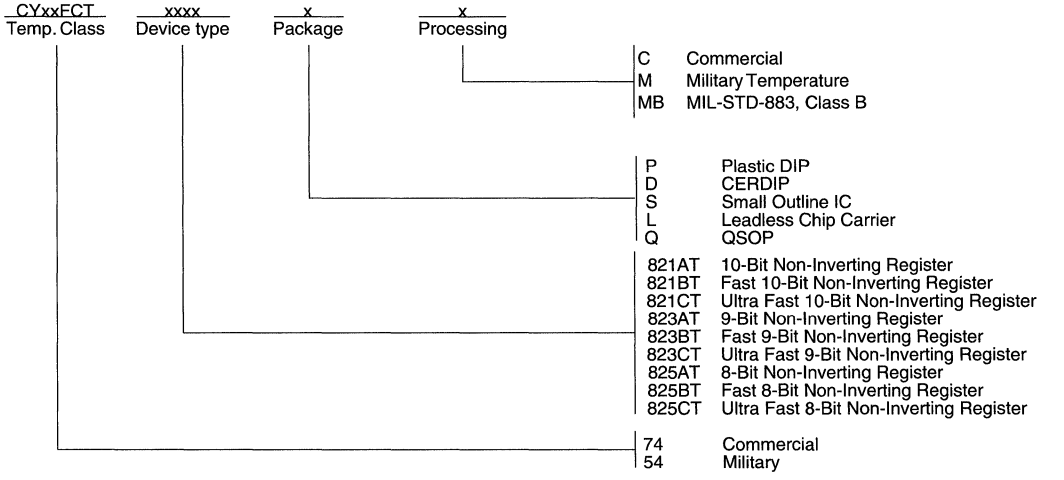
FUNCTION TABLES

Inputs					Internal Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_1	CP	Q_1	Y_1	
H	H	L	L	⌐¬	L	Z	High Z
H	H	L	H	⌐¬	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	⌐¬	L	Z	Load
H	H	L	H	⌐¬	H	Z	
L	H	L	L	⌐¬	L	L	
L	H	L	H	⌐¬	H	H	

1725 Tbl 11

H = HIGH, L = LOW, X = Don't Care, NC = No Change,
⌐¬ = LOW-to-HIGH Transition, Z = HIGH Impedance

ORDERING INFORMATION



1725 05

CY54/74FCT827T
10-BIT BUFFER

FEATURES

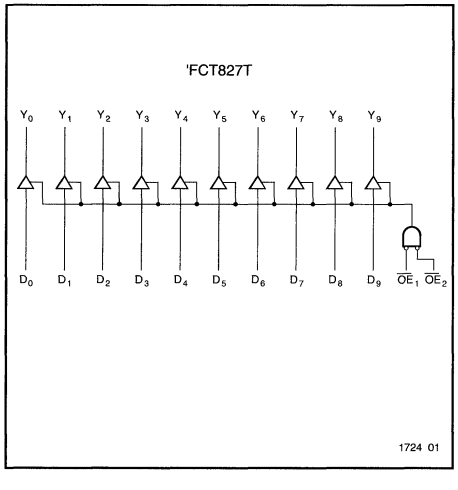
- **Function, Pinout and Drive Compatible with the FCT, F and AM29827 Logic**
- **FCT-C speed at 4.4ns max. (Com'l) FCT-A speed at 5.0ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

2

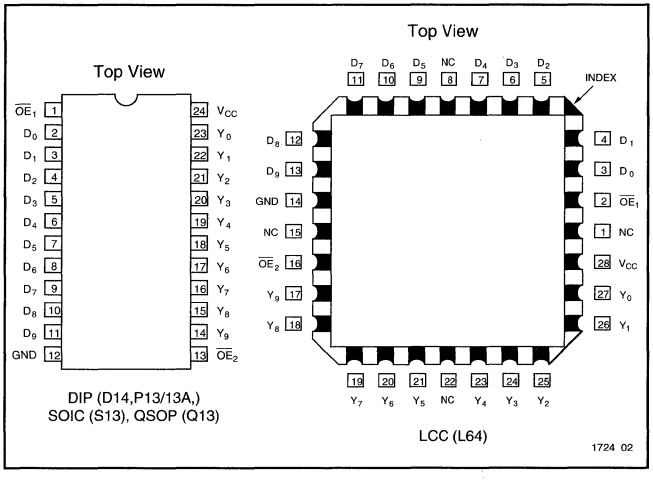
DESCRIPTION

The 'FCT827T 10-bit bus drivers provide high-performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR-ed output enables for maximum control flexibility. The 'FCT827T family of devices is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state. The 'FCT827T is non-inverting.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1724 Tbl 01

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1724 Tbl 02

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1724 Tbl 03

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1724 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1724 Tbl 05

Notes:

1. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND

1724 Tbl 06

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLES

'FCT827T (Non-Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

1724 Tbl 07

Note:
H = High, L = Low, X = Don't Care, Z = High Impedance

AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT827AT				'FCT827BT				'FCT827CT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT827T	C_L = 50pF R_L = 500Ω	–	9.0	–	8.0	–	6.5	–	5.0	–	5.0	–	4.4	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT827T	C_L = 300pF[2] R_L = 500Ω	–	17.0	–	15.0	–	14.0	–	13.0	–	11.0	–	10.0	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT828T	C_L = 50pF R_L = 500Ω	–	10.0	–	9.0	–	6.5	–	5.5	–	5.0	–	4.4	ns	1,2
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1 'FCT828T	C_L = 300pF[2] R_L = 500Ω	–	16.0	–	14.0	–	14.0	–	13.0	–	11.0	–	10.0	ns	1,2
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	–	13.0	–	12.0	–	9.0	–	8.0	–	8.0	–	7.0	ns	1,7,8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 300pF[2] R_L = 500Ω	–	25.0	–	23.0	–	16.0	–	15.0	–	15.0	–	14.0	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 5pF[2] R_L = 500Ω	–	9.0	–	9.0	–	7.0	–	6.0	–	6.7	–	5.7	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 50p R_L = 500Ω	–	10.0	–	10.0	–	8.0	–	7.0	–	7.0	–	6.0	ns	1,7,8

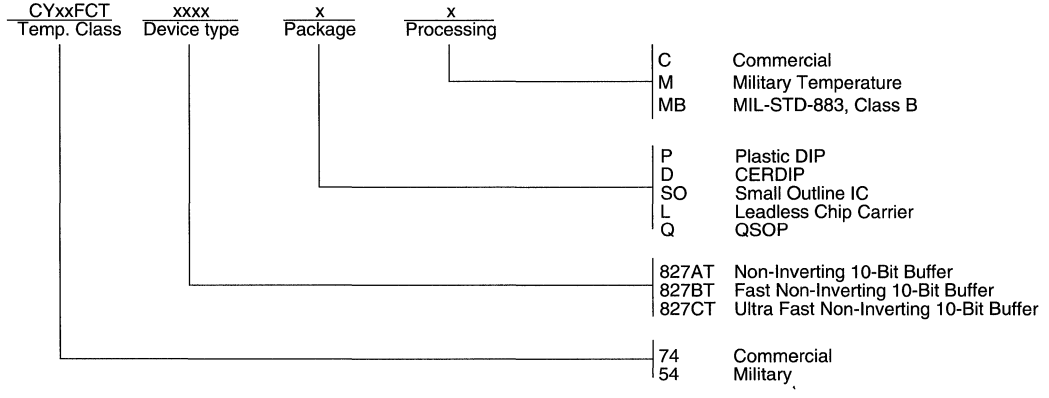
1724 Tbl 09

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



1724 03

CY54/74FCT841T
10-BIT LATCH

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F and AM29841 Logic**
- **FCT-C speed at 5.5ns max. (Com'l) FCT-B speed at 6.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Buffered Common Clear and Preset Input**
- **High Speed Parallel Latches**
- **Buffered Common Latch Enable Input**

2

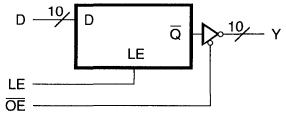
DESCRIPTION

The 'FCT841T series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/ data paths or buses carrying parity. The 'FCT841T is a buffered 10-bit wide version of the 'FCT373 function.

The 'FCT841T high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

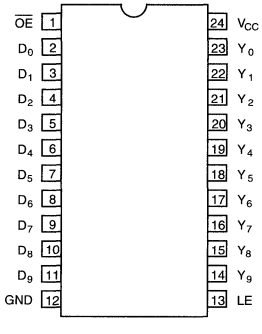
LOGIC SYMBOLS

'FCT841T (10-Bit Latch)



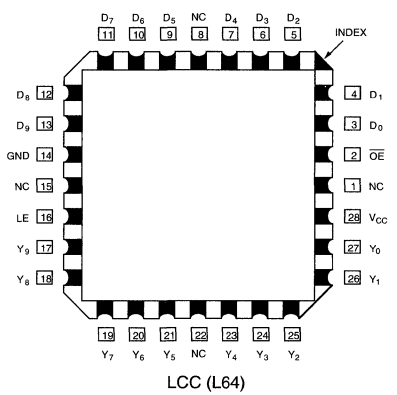
PIN CONFIGURATONS

Top View



DIP (D14,P13/13A)
SOIC (S13), QSOP (Q13)

Top View



LCC (L64)

PIN DESCRIPTION

Name	I/O	Description
D_1	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.

1719 Tbl 01

FUNCTION TABLES §

'FCT841T

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D_1	O_1	Y_1	
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	HighZ
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance. 1719 Tbl 02

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1719 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1719 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1719 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1719 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

1719 Tbl 07

Notes:

1. Typical values are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)[2]	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 2.7V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10mHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

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Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 2.7V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 2.7V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter	Test Conditions[1,*]	'FCT841AT				'FCT841BT				'FCT841CT				Units
			MIL		COM'L		MIL		COM'L		MIL		COM'L		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_I to Y_I (LE = HIGH)	C_L = 50pF R_L = 500Ω		10.0		9.0		7.5		6.5		6.3		5.5	ns
		C_L = 300pF[3] R_L = 500Ω		15.0		13.0		15.0		13.0		15.0		13.0	ns
t_{SU}	Data to LE Set-up Time	C_L = 50pF	2.5		2.5		2.5		2.5		2.5		2.5		ns
t_H	Data to LE Hold Time	R_L = 500Ω	3.0		2.5		2.5		2.5		2.5		2.5		ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_I	C_L = 50pF R_L = 500Ω		13.0		12.0		10.5		8.0		6.8		6.4	ns
		C_L = 300pF[3] R_L = 500Ω		20.0		16.0		18.0		15.5		16.0		15.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_I	C_L = 50pF R_L = 500Ω		13.0		11.5		8.5		8.0		7.3		6.5	ns
		C_L = 300pF[3] R_L = 500Ω		25.0		23.0		15.0		14.0		13.0		12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_I	C_L = 5pF[3] R_L = 500Ω		9.0		7.0		6.5		6.0		6.0		5.7	ns
		C_L = 50pF R_L = 500Ω		10.0		8.0		7.5		7.0		6.3		6.0	ns

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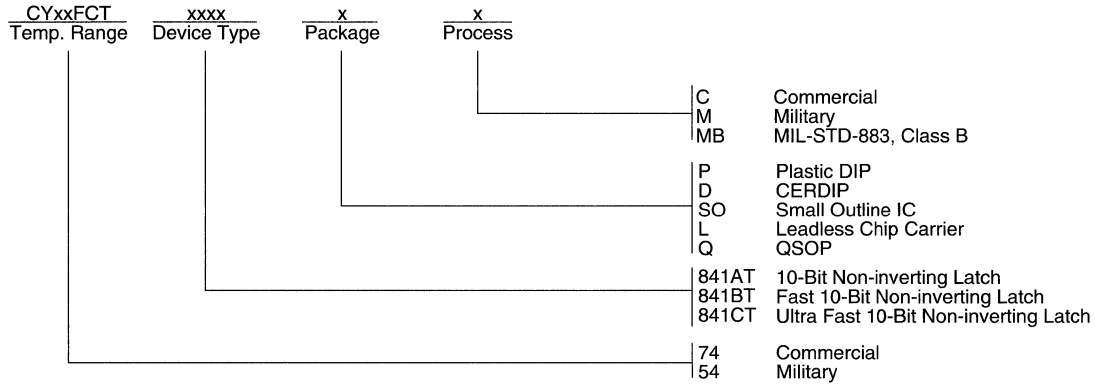
Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameters are guaranteed but not tested.

* See "Parameter Measurement Information" in the General Information Section.

ORDERING INFORMATION



CYBUS3384
DUAL 5-BIT BUS SWITCH

FEATURES

- **Zero propagation delay**
- **5Ω switches connect inputs to outputs**
- **Direct bus connection when switches are on**
- **Performs bidirectional translator function between 3.3V and 5.0V power supplies**
- **CMOS for low power dissipation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Corner power and ground pins**
- **Inputs interface with 5.0V CMOS, TTL or 3.3V CMOS**
- **Outputs interface to 5.0V TTL or 3.3V CMOS**
- **Power Down - No back Power Current**

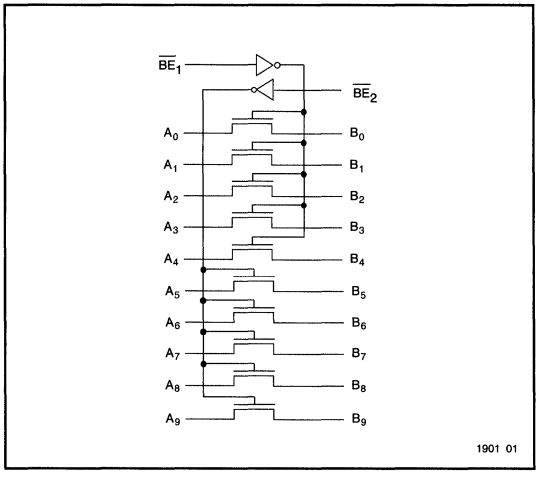
DESCRIPTION

The CYBUS3384 isa 10-bit, 2-port bidirectional bus switch that allows one bus to be connected directly to, or isolated from, another without introducing additional propagation delay or ground bounce noise. The input and output voltage levels allow direct interface with TTL and CMOS devices. Two bus enable signals, BE_1 and BE_2, turn on the upper and lower five bits, respectively.

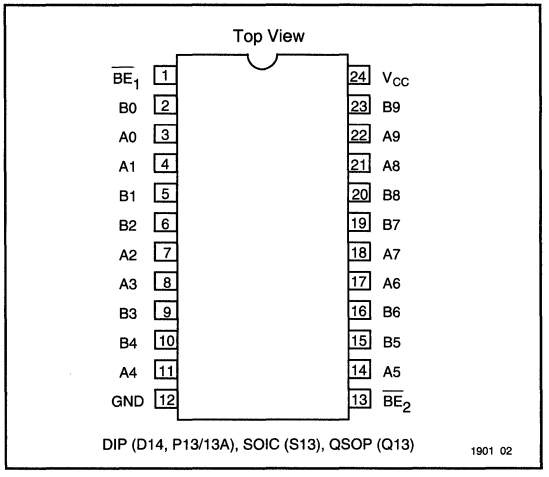
Designed to have low on resistance of 5Ω, CYBUS3384 also features POWER-OFF DISABLE making it ideal for use in systems requiring selective power down of peripherals to reduce power consumption. Additionally, CYBUS3384 facilitates bidirectional interfacing between 3.3V and 5V systems by placing a single diode in series with the 5 Volt Vcc line.

CYBUS3384 is also suitable for small signal analog applications where crosstalk and off isolation performance of -66dB at 50MHz is required.

LOGIC DIAGRAM



PIN CONFIGURATIONS



Absolute Maximum Ratings[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +165	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–20	mA

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to 7.0	V

Recommended Operating Conditions

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

2

DC Electrical Characteristics (Over recommended operating conditions)[3]

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Control Inputs Only
V_{IL}	Input LOW Voltage			0.8	V		Control Inputs Only
V_H	Hysteresis		0.2		V		Control Inputs Only
V_{IK}	Input Clamp Diode Voltage		–0.7	–1.2	V	Min	I_{IN} = –18mA
Ron	Switch On Resistance[5]		5	7	Ω	Min	V_{IN} = 0.0V, I_{ON} = 30mA
			10	15	Ω	Min	V_{IN} = 2.4V, I_{ON} = 15mA
I_{IN}	Input Leakage Current			1	µA	Max	V_{IN} = V_{CC}
I_{OZ}	Off State Current (HiZ)		0.001	1	µA	Max	V_{OUT} = 0.5V
I_{OFF}	Power-off Disable			100	µA	0V	V_{OUT} = 4.5V, V_{IN}=V_{CC}
I_{OS}	Output Short Circuit Current[4]		100		mA	Max	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[5]		6	10	pF		All Inputs
C_{OUT}	Output Capacitance[5]		6	12	pF		All Inputs

Function Table

$\overline{BE}_1$	$\overline{BE}_2$	B0-4	B5-9	Function
H	H	Hi-Z	Hi-Z	Disconnect
L	H	A0-4	Hi-Z	Connect
H	L	Hi-Z	A5-9	Connect
L	L	A0-4	A5-9	Connect

Pin Description

Name	I/O	Function
A0-9	I/O	Bus A
B0-9	I/O	Bus B
$\overline{BE}_1$, $\overline{BE}_2$	I	Bus Switch Enable

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.
6. Measured by voltage drop between A and B pin at indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A,B) pins.

Power Supply Characteristics

Symbol	Parameter	Min	Typ[3]	Max	Units	TEST Conditions[7]
I_{cc}	Quiescent Power Supply Current	–	–	1.5	mA	V_{CC} = MAX, V_{IN} = GND or Vcc, f = 0
ΔI_{cc}	Power Supply Current/Input High[8]	–	–	2.5	mA	V_{CC} = MAX, Input = 3.4V, f = 0 Per control input
Q_{ccd}	Dynamic Power Supply Current per MHz[9]	–	–	0.30	mA/MHz	V_{CC} = MAX, A & B pins open Control input toggling @ 50% duty cycle
I_c	Total Power Supply Current[10, 11]	–	–	9.0	mA	V_{CC} = MAX, A & B pins at 0.0V Control input toggling @ 50% duty cycle V_{ih} = 3.4V, f clock = 10 MHz

Notes:

7. For conditions shown as MIN or MAX use the appropriate values specified under DC specifications.

8. Per TTL-driven input (Vi=3.4V, control inputs only). A and B pins do not contribute to Icc.

9. This current applies to the control inputs only and represents the current required to switch internal capacitance at the specified frequency. The A and B inputs generate no significant AC or DC currents as they transition. This parameter is not tested but is guaranteed by design.

10. Ic = I Quiescent + I Inputs + I Dynamic
    Ic = Icc+ ΔIccDhNt + Occd (fiNi)
    Icc = Quiescent Current
    ΔIcc = Power Supply Current for each TTL HIGH input (Vi = 3.4V, control inputs only)
    Dh = Duty Cycle for each TTL input that is HIGH (control inputs only).
    Nt = Number of TTL inputs that are at DH (control inputs only).
    fi = frequency that the inputs are toggled (control inputs only).

11. Note that activity on A and/or B inputs do not contribute to Ic if A and B inputs are between gnd and 7.0V. The switches merely connect and pass through activity on these pins. For example: if the control inputs are at 0V and the switches are on, Ic will be equal to Icc only regardless of activity on the A and B pins.

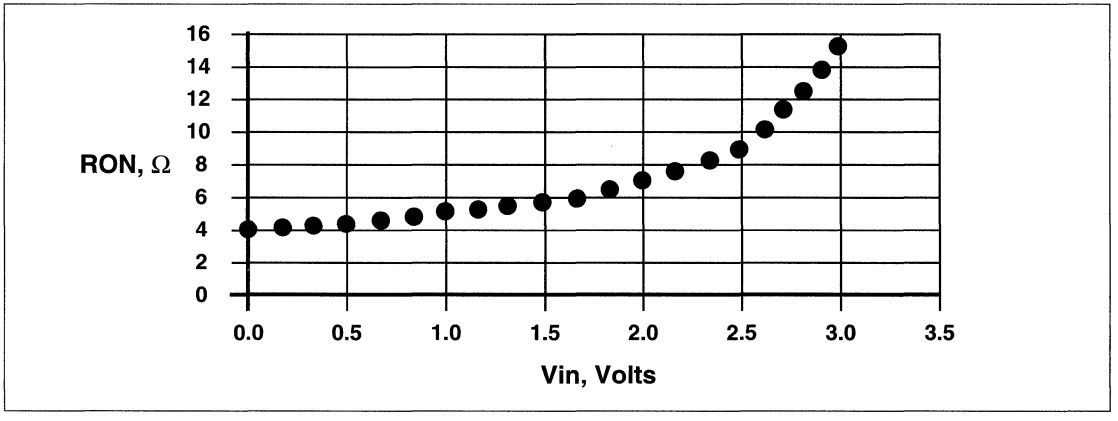


Figure 3. On Resistance vs Vin @ 4.75 Vcc

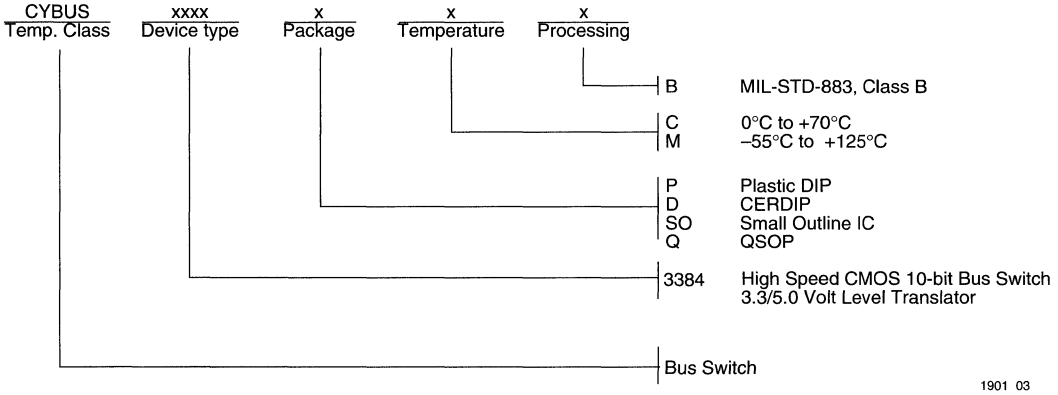
SWITCHING CHARACTERISTICS

Commercial TA = 0° to 70°C, Vcc = 5.0V±5%. Military TA = –55° to 125°C, Vcc = 5.0V±10%.
Cload = 50pF, Rload = 500Ω, unless otherwise noted.

Symbol	Description	Note	COM'L		Military		Units
			Min.[13]	Max.	Min.[1]	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay Ai to Bi, Bi to Ai	14,15		0.25		0.25	ns
t_{PZH} t_{PZL}	Switch Turn On Delay BEA, BEB to Ai, Bi	13	1.5	6.5	1.5	7.5	ns
t_{PHZ} t_{PLZ}	Switch Turn Off Delay BEa, BEB to Ai, Bi	13,14	1.5	5.5	1.5	6.5	ns
$\lvert Q_{ci} \rvert$	Charge Injection, Typical	16,17		1.5		1.5	pC

Notes:
13. See Test Circuit and Waveforms. Minimums guaranteed but not tested.
14. This parameter is guaranteed by design but not tested.
15. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch is of the order of 0.25 ns for 50 pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
16. Measured at switch turn off, A to C, load = 50 pF in parallel with 10 meg scope probe, Vin at A = 0.0 volts.
17. Characterized parameter. Not 100% tested.

ORDERING INFORMATION



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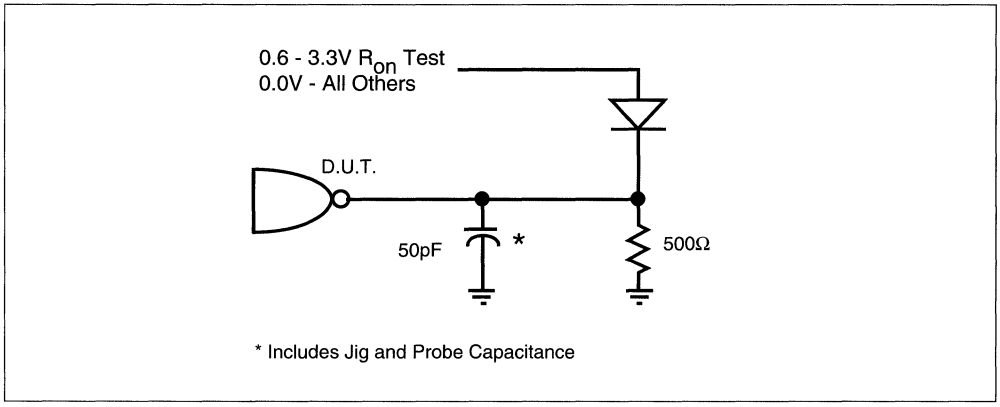


Figure 4. Test Load

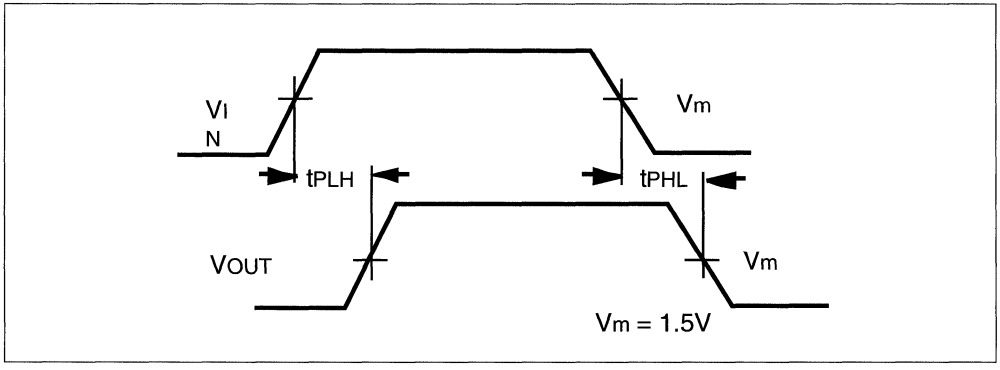


Figure 5. Waveforms for Non-Inverting Functions

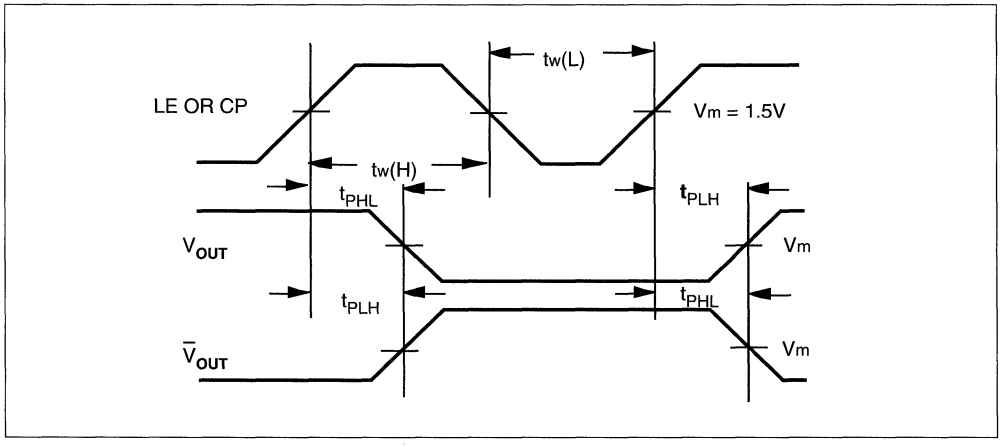


Figure 6. Propagation Delays from Rising-Edge Clock or Enable

1901 05

APPLICATION INFORMATION

CYBUS3384 is a 10 channel bidirectional solid state bus switch with a "near zero" propagation delay.

The CYBUS3384 is organized into two groups of five N-channel MOSFET's, each group has an independent control input for output enable (see Figure 7). Because the N-channel MOSFET is physically symmetric, the device is naturally bidirectional and therefore each N-channel device pin can act as input or output.

The two enable inputs ($\overline{BE}_1$ and $\overline{BE}_2$) sense TTL level signals and drive the gates of the N-channel MOSFET's to Vcc. With the gate at Vcc, the output voltage will follow the input voltage up to Vcc minus the threshold voltage. At this point the N-channel MOSFET begins to turn off rapidly increasing the effective resistance (Ron) such that further increases to input voltage no longer increase the output voltage (see Figure 8).

When either the input or output of the 3384 is near zero volts and the gate is at Vcc, the device is fully on, (low resistance) and available to pass large currents in either direction. In this condition, the 3384 inputs are directly connected to the outputs.

The 3384 provides no signal drive itself. As a result the rise and fall times of the 3384 outputs are determined by the device driving the 3384 inputs rather than the 3384 itself.

The propagation delay contributed by the 3384 is essentially zero when the N-channel gate is at Vcc.

When the device is unpowered, the 3384 draws no current from the I/O or control inputs, and there is no current path fromthe I/O or control pins to the power pins. There is no back power or current drain problems when the device is unpowered.

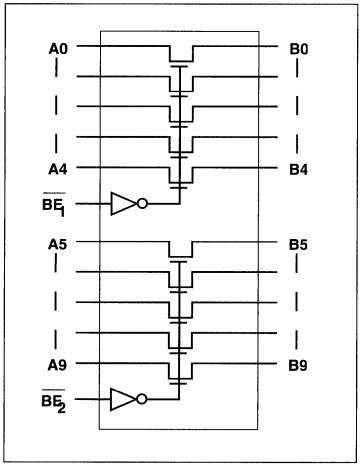


Figure 7. P74FCT3384

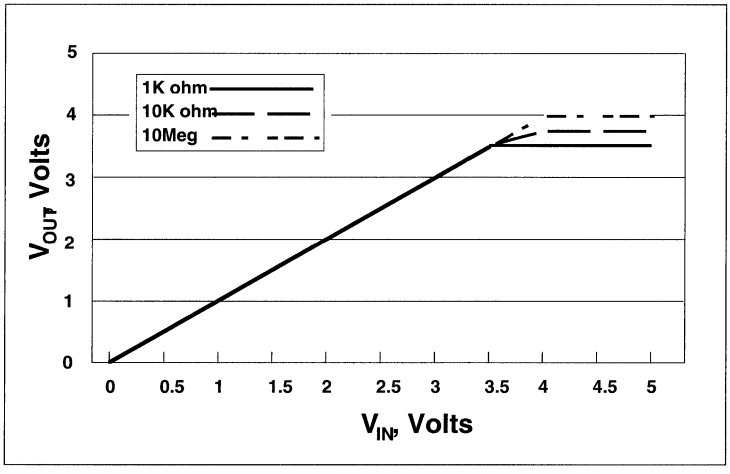


Figure 8. Vout vs Vin

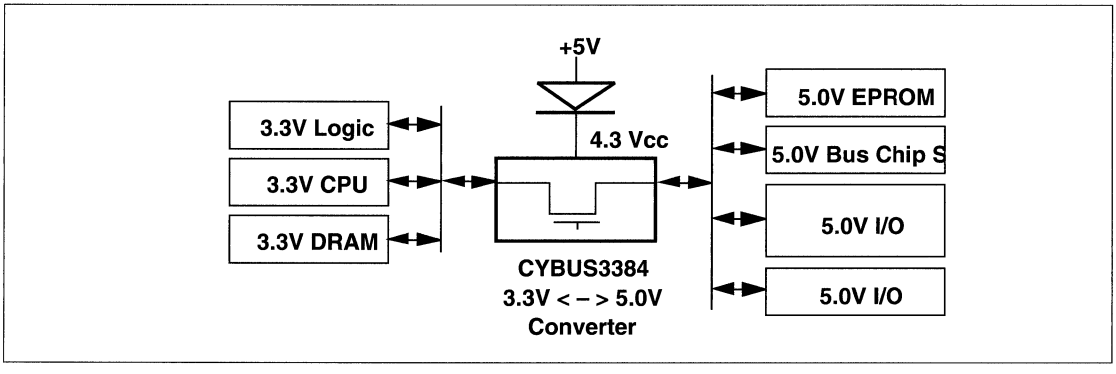


Figure 9. System with CYBUS3384 as 5V TTL to 3V Converter

APPLICATION INFORMATION

The 3384 provides an ideal interface between 5 volt and 3.3 volt components. Because the 3384 provides no signal drive, the ICC demands are small, limited to AC switching of the N- channel gates, control circuitry and a minute amount of I/O leakage. Since the small current demands of the 3384, it is possible to lower the 3384 VCC from a standard 5.0 volt supply with a small inexpensive diode and provide a low current full bidirectional signal compatability between the older 5 volt logic family signals and the newer 3.3 volt logic family signals.

By adding a diode the 3384 VCC supply voltage can be shifted to 4.3 volts as shown in Figure 9. 5 volt signals will now be limited to 3.3 volts as they pass through the 3384. 3.3 volt signals will pass back through the 3384 unaltered and provide compatability with 5 volt TTL input requirements. Note that the conversion is bidirectional and is limited to 3.3 volts independent of which side is driven to 5 volts. The 3384 could convert 5 volt signals for use on a 3.3 volt bus or convert a 5 volt bus to signals compatable with 3.3 volt components.

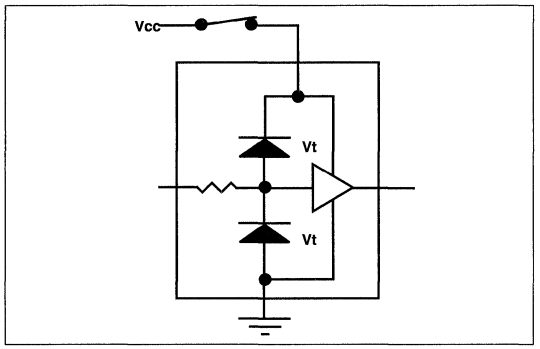


Figure 10. Gate Input (Power ON)

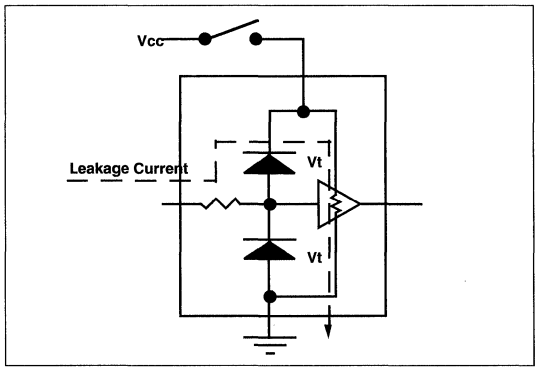


Figure 11. Gate Input (Power OFF)

3.3V/5V Supply Operation

In certain system applicaitons, the CYBUS3384 must operate from either a 5 volt or 3.3 volt power supply, depending on the state of the system. If this occurs, the circuit shown in Figure 12 can be added to step the 3.3V supply up to a nominal 5 volt level. The low-cost, high-efficiency Step Up regulator shown in the figure is available from Linear Technology, Maxim, and other suppliers. The diode arrangement will automatically select the active supply. Standard silicon diodes can be used because the CYBUS3384 Vcc minimum is specified at 4.0V.

Low Power Bus Isolation

Modern battery-operated systems rely on internal power management schemes to disconnect power from subsystems not in use. Usually the subsystem bus input ESD protection circuits consist of a pair of clamp diodes to limit input voltage excursions to a maximum of Vcc +Vt and –Vt (see Figure 10). Removing power from these circuits causes the Vcc ESD clamp diode to connect the dead circuit inputs to gnd, often significantly increasing bus loading and power dissipation (see Figure 11). The CYBUS3384 placed on the input of the load to be disconnected effectively prevents bus loading and its associated problems.

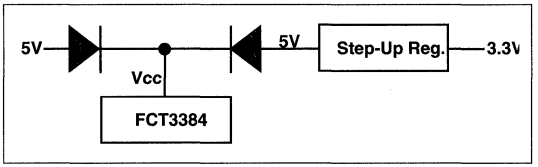


Figure 12. 3.3V/5V Supply Switch

High Speed Dual Port RAM

As shown in Figure 13, a high-speed, dual-port memory is implemented using a combination of commodity SRAM, a simple arbitration circuit, and the CYBUS3384. Processor 1 is the system host processor while Processor 2 is a dedicated peripheral processor (such as a DSP for acquisitioning and manipulating data). Either processor can own the SRAM by first reading the BUSY bit to determine if the SRAM is available. If so, the requesting processor takes control by writing the OWN bit (which redirects the bus through the CYBUS3384s and sets the BUSY bit notifying the other bus the SRAM is not available). Processor 1 owns the bus and may now access the SRAM as needed. When finished, Processor 1 resets the OWN bit releasing the SRAM. The SRAM access sequence is identical for Processor 2. In this application, the CYBUS3384 saves 10ns compared to using an F244 address buffer and an F245 data bus transceiver. This, in turn, allows the use of a slower, more available SRAM, resulting in system cost and power savings.

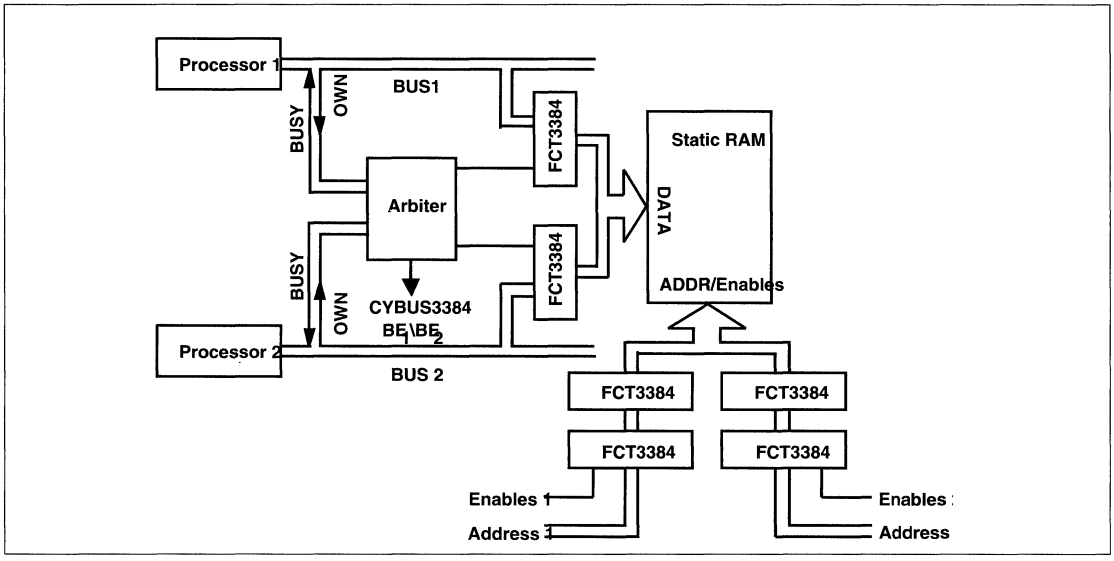


Figure 13. High Speed Dual Port RAM

Selectable Termination Loads

In some applications, it is desirable to vary the characteristic termination impedance as the system configuration changes. This is a common problem in automatic test equipment applications. Because of their low ON resistance, miniature relays are often used to switch termination loads. A single CYBUS3384 can replace as many as 10 such relays resulting in faster switching operation, lower power, and significant cost savings

Fast Latch

Figures 14 and 15 show variations of a latch having a sub 1ns progagational delay time using the CYBUS3384 in combination with other components This circuit has the advantage of being four to ten times faster than an equivalent implementation using a 373 latch – and with no added noise. Figure 14 relies on the stray capacitance of the bus to maintain data when the CYBUS3384 opens. Assuming 50pF stray capacitance at room temperature and a 1 microampere input leakage current, a 1 volt "droop" from the initial voltage level would take 50 microseconds. Figure 15 shows the addition of a physical capacitor if there is insufficient stray capacitance. Figure 16 shows an active bus termination capable of sustaining the programmed logic an indefinite period of time in the presence of Vcc.

Conclusion

The CYBUS3384 is a versatile, high-speed connect device that can solve a multitude of circuit connect problems. It is a compact, low-cost solution that offers improved timing margins and low-noise operation.

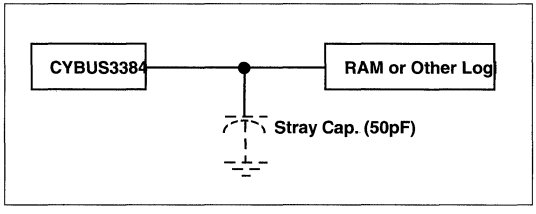


Figure 14. Latch Variation With Stray Capacitance

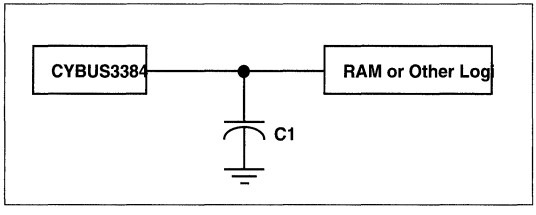


Figure 15. Latch Variation With Physical Capacitor

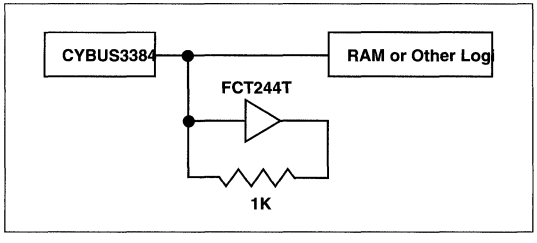


Figure 16. Active Bus Termination

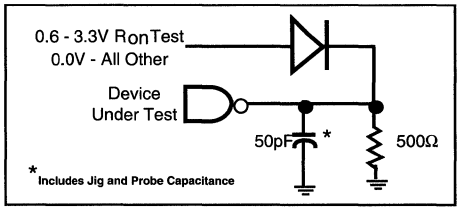


Figure 1. Test Load

The 'FCT3384 allows direct connection of 3V system busses and 5V system busses with zero delay between them. The circuit used is shown in Figure 4 and requires only the 'FCT3384 and a single diode placed between the 5V power supply and the Vcc pin on the 'FCT3384.

Switch Off

When the control input BEn is HIGH, the two sides of the switch are completely isolated. Irrespective of the Vcc on the 'FCT3384, either side of the switch may be driven up to 7V with minimal leakage occurring (typically <<1μA) because there are no parastic diodes on the I/Os.

Switch On

When the control input $\overline{BEn}$ is low, the two sides of the switch are directly connected through the N channel transistor which will produce a very small (typically 0.25ns) propagation delay through the 'FCT3384. This delay is capacitive load on the other side of the switch. (Note: the 'FCT3384 differs from conventional chips in that it has no output drivers so that whatever the Vcc on the 'FCT3384, the undriven side of the switch can never be higher than the driven side.)

In the circuit suggested, either side of the switch may be riven up to 7V, but the voltage on the undriven side of the switch will not go above about 3.3V. This behaviour can be represented by the diagram shown in Figure 5.

In the data sheet the actual behaviour of the device is given and the voltage on the undriven side of the switch is defined in terms of the voltage that must be applied across the N channel transistors "gate" and "source" terminals (Vgs) for the transistor to remain on. Typically this is about 1V. Since the transistor is totally symmetrical, either side A or side can be regarded as the "source." If the voltage on the undriven side attempts to go above the value necessary to maintain the Vgs, then the transistor begins to turn off and this is shown in the Ron vs Vin curve in the data sheet.

The gate voltage is about the same as the Vcc applied to the 'FCT3384. In this application, with the diode in the power supply line, the Vcc is about 4.3V, so the voltage in the undriven side of the switch can never go above Vcc -Vgs -1V = 3.3V regardless of the voltage on the driven side of the switch, as shown in Figure 6.

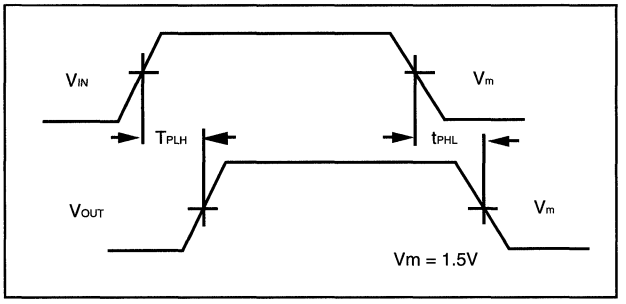


Figure 2. Waveform for A to B path

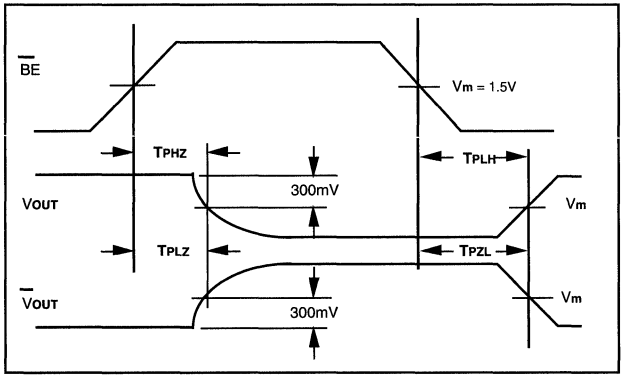


Figure 3. Propagation delays from bus enable

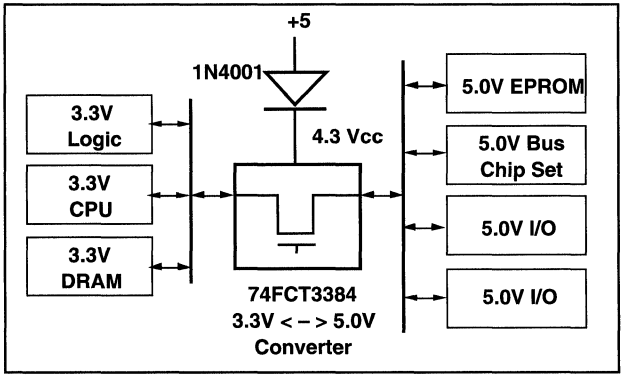


Figure 4. Example of 'FCT3384 circuit

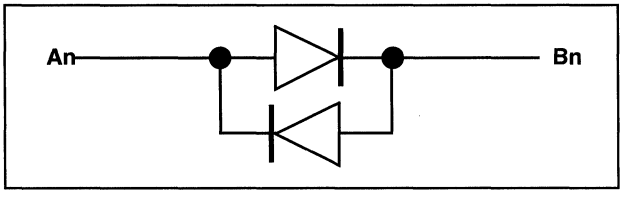


Figure 5. Switch voltage control

FCT2–T (25Ω Outputs)

CY54/74FCT2240T
CY54/74FCT2244T
8-BIT BUFFERS/LINE DRIVERS

FEATURES

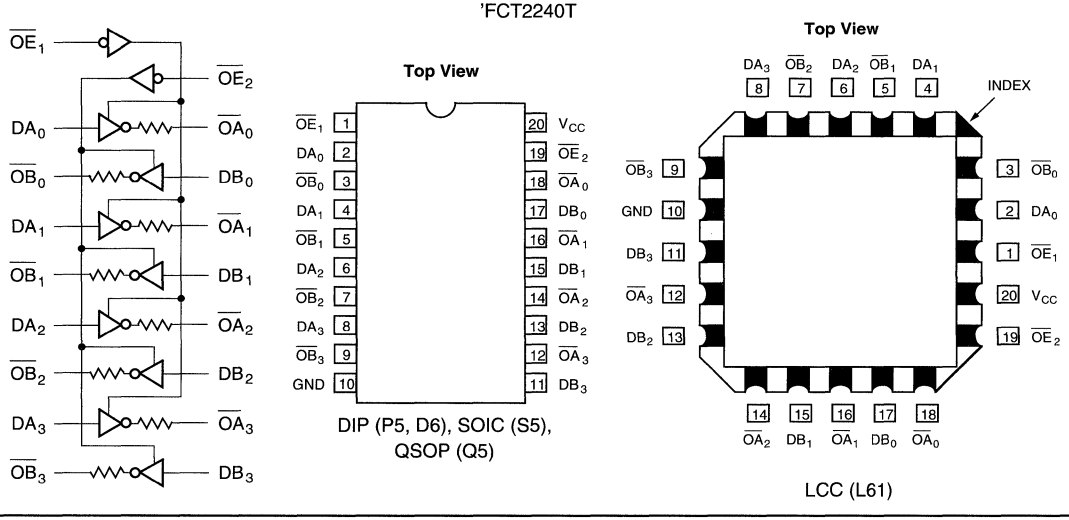
- **Function and pinout compatible with the FCT and F Logic**
- **25Ω Output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.1ns max. (Com'l), FCT2244T FCT-A speed at 4.8ns max. (Com'l)**
- **TTL output level versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Fully compatible with TTL input and output logic levels**
- **12mA Sink Current (Commercial), 12mA (Mil) 15mA Source Current (Commercial), 12mA (Mil)**
- **3-State Outputs**

DESCRIPTION

'FCT2240T and 'FCT2244T are octal buffers and line drivers that include on-chip 25Ω terminating resistors at each of the outputs, to minimize noise resulting from reflections or standing waves in high-performance applications. The on-chip resistors reduce overall board space and component count.

Designed to be employed as memory address drivers, clock drivers, and bus-oriented transmitters/receivers, the devices provide speed and drive capabilities commensurate with their fastest bipolar logic counterparts while reducing overall power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without the need for external components.

FUNCTIONAL BLOCK DIAGRAM and PIN CONFIGURATIONS



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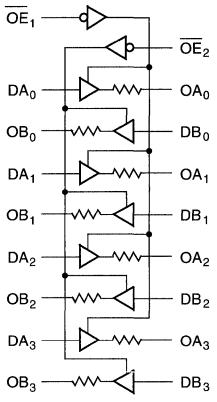
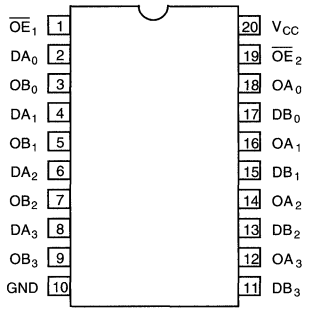
FUNCTIONAL BLOCK DIAGRAM and PIN CONFIGURATIONS

'FCT2244T

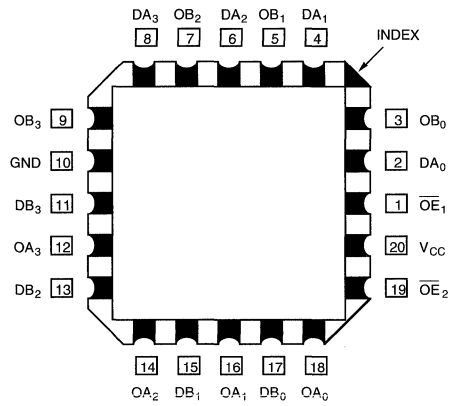


Top View



DIP (P5, D6), SOIC (S5),
QSOP (Q5)

Top View



LCC (L61)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[5]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Short should not exceed one second. To minimize internal chip heating and more accurately reflect operational values, use of high-speed test apparatus and/or sample and hold techniques are preferable. Otherwise prolonged shorting of a high output may raise chip temperature well above normal causeing invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current [9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1 = \overline{OE}_2$ = GND, $OE_2 = V_{CC}$, V_{IN} = 3.4V or V_{IN} = GND

TRUTH TABLES

'FCT2240T

Inputs			Output
$\overline{OE}_1$	$\overline{OE}_2$	D	
L	L	L	H
L	L	H	L
H	H	X	Z

'FCT2244T

Inputs			Output
$\overline{OE}_1$	OE_2	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High Impedance

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

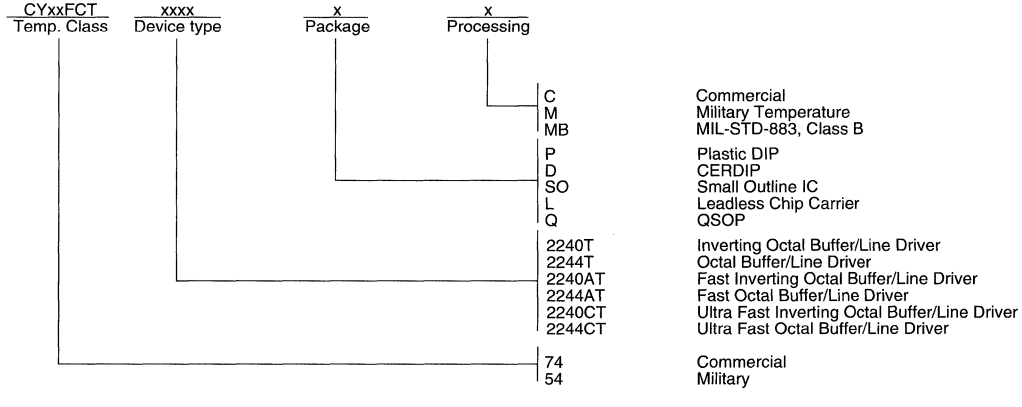
Symbol	Parameter	'FCT2240T				'FCT2240AT				'FCT2240CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	-	-	1.5	4.1	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	-	-	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	-	-	1.5	5.2	ns	

AC CHARACTERISTICS

Symbol	Parameter	'FCT2244T				'FCT2244AT				'FCT2244CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	7.0	1.5	6.5	1.5	5.1	1.5	4.8	-	-	1.5	4.3	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	8.5	1.5	8.0	1.5	6.5	1.5	6.2	-	-	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	7.5	1.5	7.0	1.5	5.9	1.5	5.6	-	-	1.5	5.2	ns	

10. Minimum limits are guaranteed but not tested on Propagation Delays.
*Refer to the 'Parameter Measurement Information' section in this book.
AC Characteristics guraranteed with C_L = 50pF.

ORDERING INFORMATION



CY54/74FCT2245T
8-BIT TRANSCEIVER

FEATURES

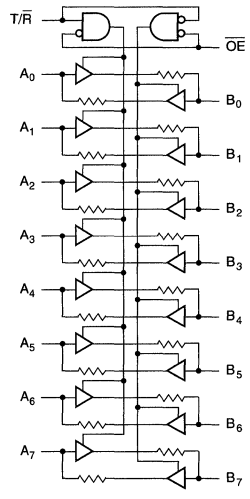
- **Function and pinout compatible with FCT and F Logic**
- **25Ω Output Series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.1ns max. (Commercial) FCT-A speed at 4.6ns max. (Commercial)**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12mA Sink Current (Com'l), 12mA (Mil) 15mA Source Current (Com'l), 12mA (Mil)**
- **3-State Outputs**

DESCRIPTION

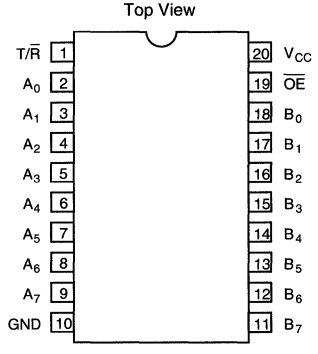
The 'FCT2245T contains eight noninverting, bidirectional buffers with 3-state outputs intended for bus oriented applications. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. For this purpose, the 'FCT2245T can be used in an existing design to replace the 'FCT245T. For the 'FCT2245T current sinking capability is 12mA at the A & B ports.

The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (Active HIGH) enables data from A ports to B ports; receive (Active LOW) enables data from B ports to A ports. The output enable ($\overline{OE}$), input, when HIGH, disables both the A and B ports by putting them in a high Z condition.

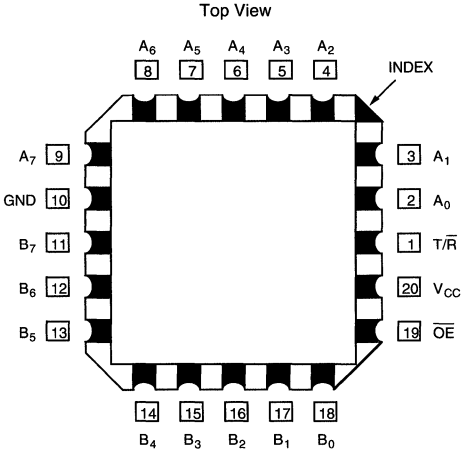
LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP (P5, D6), SOIC (S5), QSOP (Q5)



LCC (L61)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[5]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.50	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.50	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the values set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, T/$\overline{R}$ = $\overline{OE}$ = GND, Outputs Open, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[9]	2.0	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.3	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND
		3.5	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.5	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, T/$\overline{R}$ = $\overline{OE}$ = GND and V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These values are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

AC CHARACTERISTICS

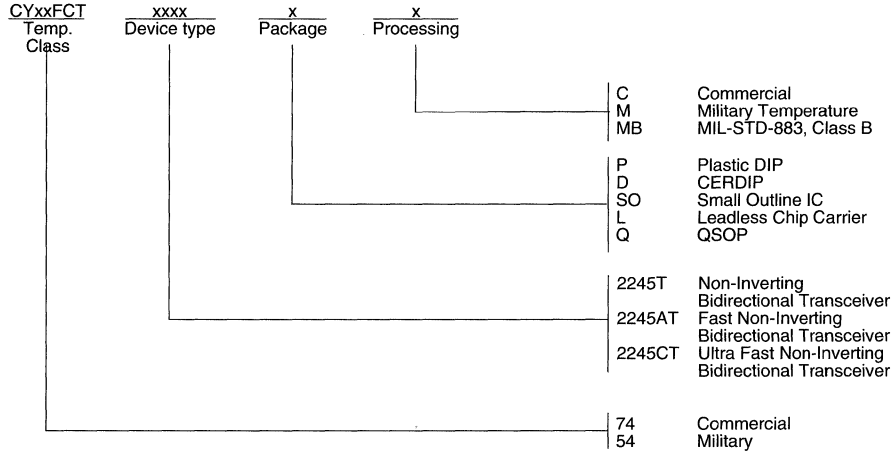
Symbol	Parameter	'FCT2245T				'FCT2245AT				'FCT2245CT		UNITS	Fig. No.*
		MIL		COM'L		MIL		COM'L		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.5	7.5	1.5	7.0	1.5	4.9	1.5	4.6	1.5	4.1	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.0	1.5	9.5	1.5	6.5	1.5	6.2	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.5	ns	

Note:

10. Minimum limits are guaranteed but not tested on Propagation Delays.
    AC Characteristics guaranteed with C_L = 50pF.

* Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION



CY54/74FCT2257T
QUAD 2-INPUT MULTIPLEXER

FEATURES

- **Function and pinout compatible with the FCT and F logic**
- **25Ω Output series resistors to reduce transmission line reflection noise.**
- **FCT-C speed at 4.3ns max. (Commercial) FCT-A speed at 5.0ns max. (Commercial)**
- **TTL output level versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Fully compatible with TTL input and output logic levels**
- **12mA Sink Current (Commercial), 12mA (Mil) 15 mA Source Current (Commercial), 12mA (Mil)**
- **3-State Outputs**

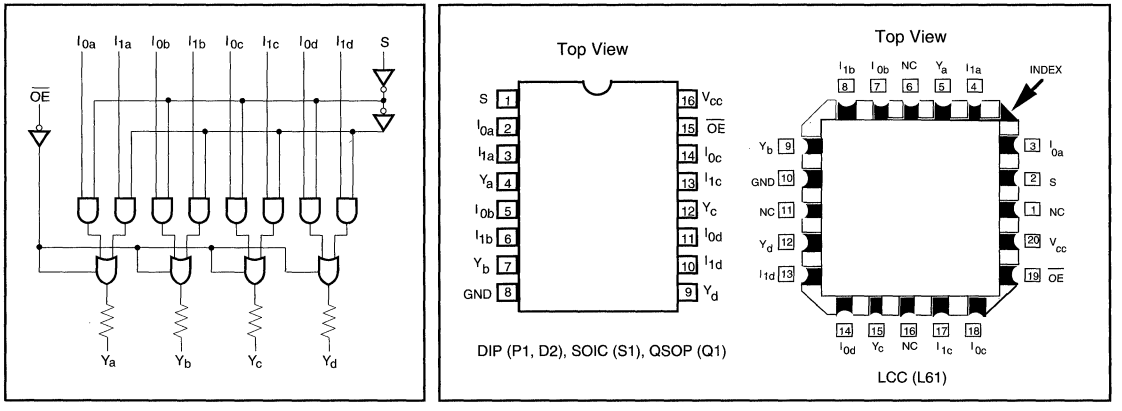
DESCRIPTION

The 'FCT2257T has four identical 2-input multiplexers with 3-state outputs that select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the select input is HIGH. Data appears at the output in true noninverted form for the 'FCT2257T. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2257T can be used to replace the 'FCT257T to reduce noise in an existing design.

The 'FCT2257T is a logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the select input. Outputs are forced to a high-impedance "OFF" state when the Output Enable input ($\overline{OE}$) is HIGH.

All but one device must be in the high-impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond thevalues set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Input Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		1.7	4.0[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.7	8.0[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

FUNCTION TABLE

Inputs				Output
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance (OFF) state

DEFINITION OF FUNCTIONAL TERMS

Pins	Description
$I_{0n} - I_{1n}$	Data inputs
S	Common select input
$\overline{OE}$	Enable input (Active-Low)
$Y_a - Y_d$	Data outputs 'FCT2257T

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Sym.	Parameter	'FCT2257T				'FCT2257AT				'FCT2257CT		Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Prop Delay I_{na}, I_{nb} to Y_n	1.5	7.0	1.5	6.0	1.5	5.8	1.5	5.0	1.5	4.3	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay S to O_n	1.5	12.0	1.5	10.5	1.5	8.1	1.5	7.0	1.5	5.2	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time to High or Low	1.5	10.0	1.5	8.5	1.5	8.0	1.5	7.0	1.5	6.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time from High or Low	1.5	8.0	1.5	6.0	1.5	5.8	1.5	5.5	1.5	5.0	ns	1, 7, 8

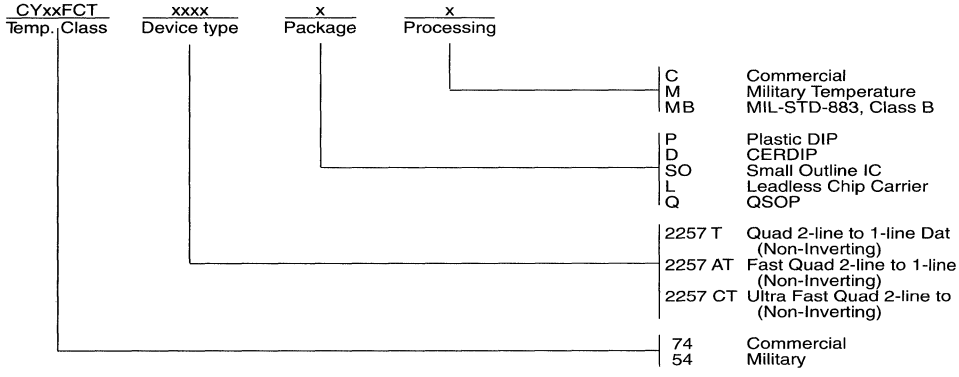
Note

10. Minimum limits are guaranteed but not tested on propagation delays.

* AC characteristics guaranteed with C_L = 50pF.

*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION



CY54/74FCT2373T
CY54/74FCT2573T
8-BIT LATCHES

FEATURES

- **Function and pinout compatible with the fastest bipolar logic**
- **25Ω output series resistors to reduce transmission line reflection noise**
- **FCT-C speed at 4.7ns max. (Commercial) FCT-A speed at 5.2ns max. (Commercial)**
- **Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Power-off disable feature**
- **Matched rise and fall times**
- **Fully compatible with TTL input and output logic levels**
- **12mA sink current (Commercial), 12mA (Mil) 15mA source current (Commercial), 12mA (Mil)**

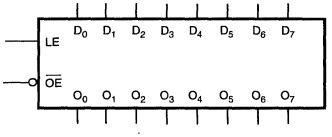
DESCRIPTION

The 'FCT2373T and 'FCT2573T are 8-bit, high-speed CMOS TTL-compatible buffered latches with 3-state outputs that are ideal for driving high-capacitance loads, such as memory and address buffers. On-chip 25Ω termination resistors have been added to the outputs to reduce system noise caused by reflections. 'FCT2373T can be used to replace 'FCT373, and 'FCT2573T to replace 'FCT573 to reduce noise in an existing design. 'FCT2573T is identical to 'FCT2373T except that all inputs are on one side of the package and the outputs on the other side.

When latch enable (LE) is high, the flip flops appear transparent to the data. Data that meets the required set-up times are latched when LE transitions from HIGH to LOW. Data appears on the bus when the output enable ($\overline{OE}$) is LOW. When output enable is HIGH, the bus output is in the high impedance state. In this mode, data can still be entered into the latches.

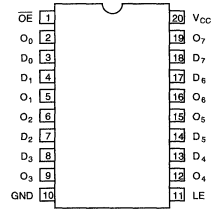
LOGIC SYMBOL

'FCT2373T & 'FCT2573T



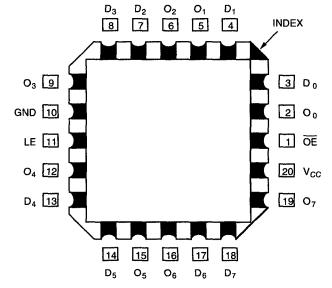
PIN CONFIGURATIONS

TOP VIEW



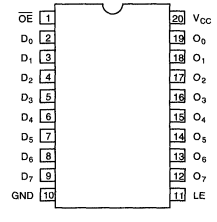
DIP(P5,D6), SOIC (S5), QSOP (Q5)

'FCT2373T TOP VIEW



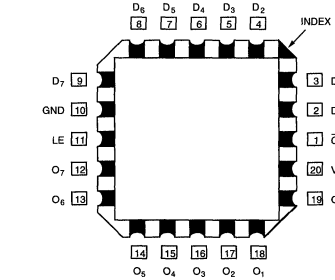
LCC (L61)

TOP VIEW



DIP P5, D6),SOIC(S5), QSOP (Q5)

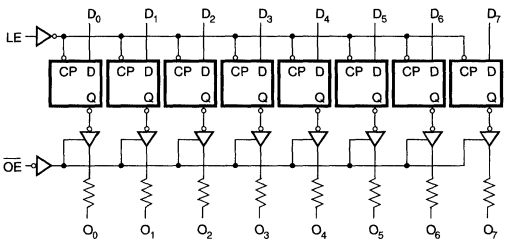
'FCT2573T TOP VIEW



LCC (L61)

LOGIC DIAGRAMS

'FCT2373T - 'FCT2573T



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	28	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \leq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C
Supply Voltage (V_{CC})	**Min**	**Max**
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

FUNCTION TABLES (Each Latch)

Inputs			Outputs 'FCT2373T/'FCT2573T
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = HIGH Impedance
Q_0 = previous state of flip flops (Q_{n-1})

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS ('FCT2373T — 'FCT2573T)

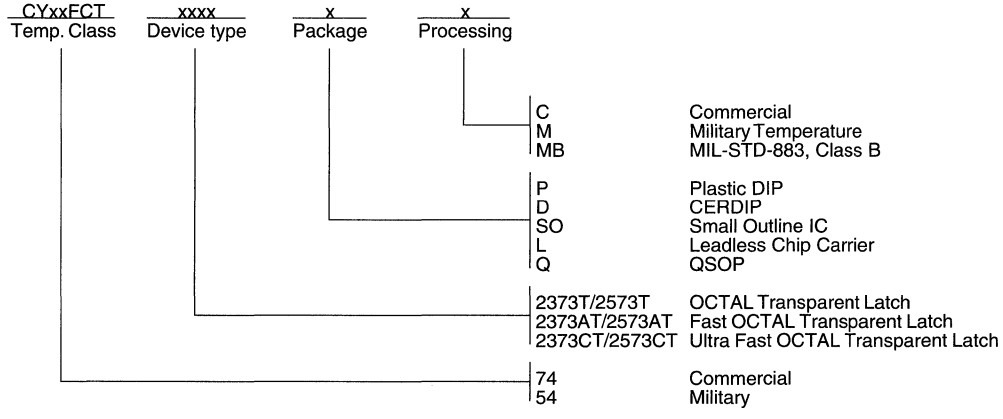
Sym.	Parameter	'FCT2373T 'FCT2573T				'FCT2373AT 'FCT2573AT				'FCT2373CT 'FCT2573CT				Units	Fig. No*.
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Prop Delay D_n to O_n	1.5	8.5	1.5	8.0	1.5	5.6	1.5	5.2	1.5	5.1	1.5	4.7	ns	1, 3
t_{PLH} t_{PHL}	Prop Delay LE to O_n	2.0	14.0	2.0	13.0	2.0	9.8	2.0	8.5	2.0	8.0	2.0	6.9	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	12.5	1.5	11.0	1.5	7.5	1.5	6.5	1.5	6.3	1.5	6.2	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.5	1.5	7.0	1.5	6.5	1.5	5.5	1.5	5.9	1.5	5.0	ns	
$t_s(H)$ $t_s(L)$	Setup Time, High to Low D_n to LE	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	ns	9
$t_n(H)$ $t_n(L)$	Hold Time, High to Low D_n to LE	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns	
$t_w(H)$	LE Pulse Width High	6.0	–	6.0	–	6.0	–	5.0	–	6.0	–	5.0	–	ns	5

Notes:

10. Minimum limits are guaranteed but not tested on Propagation Delays.

*Refer to the 'Parameter Measurement Information' section in this book. AC Characteristics guaranteed with C_L = 50 pF.

ORDERING INFORMATION



CY54/74FCT2374T
CY54/74FCT2574T
8-BIT REGISTERS

FEATURES

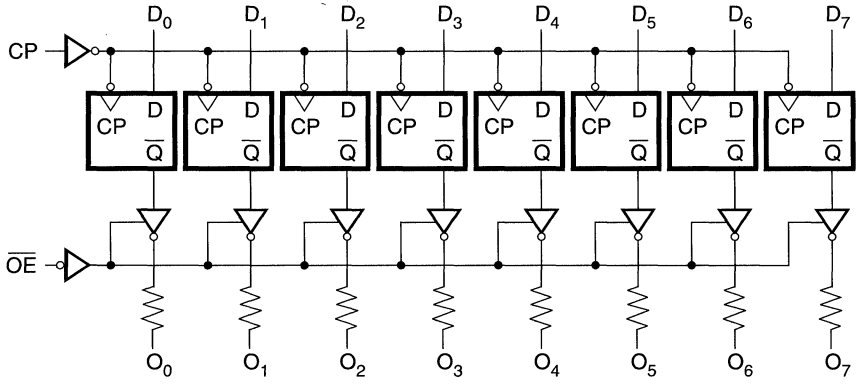
- Function and pin compatible with FCT & F logic
- 25Ω output series resistors to reduce transmission line reflection noise
- FCT-C speed at 5.2ns max. (Commercial) FCT-A speed at 6.5ns max. (Commercial)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 12 mA sink current (Commercial), 12 mA (Mil) 15 mA source current (Commercial), 12 mA (Mil)
- Edge Triggered D Type Inputs
- 250 MHz Typical Toggle Rate
- Buffered Positive Edge Triggered Clock

DESCRIPTION

The 'FCT2374T and 'FCT2574T are high-speed low power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2374T and 'FCT2574T can be used to replace the 'FCT374T and 'FCT574T to reduce noise in an existing design. Both devices have 3-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The 'FCT2574T is identical to 'FCT2374T except that all the outputs are on one side of the package and inputs on the other side. The flip-flops contained in the 'FCT2374T and 'FCT2534T will store the state of their individual D inputs that meet the setup and hold time requirements on the low-to-high clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high-impedance state. The state of output enable does not affect the state of the flip-flops.

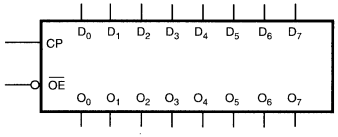
LOGIC DIAGRAM

'FCT2374T - 'FCT2574T



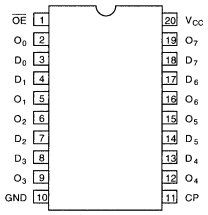
LOGIC SYMBOL

'FCT2374T - 'FCT2574T



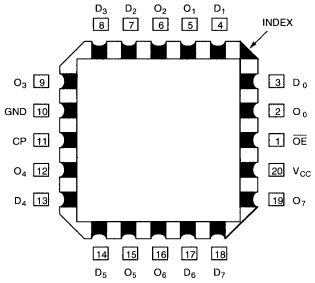
PIN CONFIGURATIONS

Top View



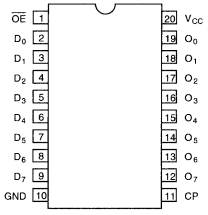
DIP(D6, P5), SOIC (S5), QSOP (Q5)

'FCT2374T **Top View**



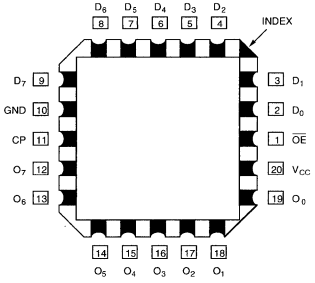
LCC(L61)

Top View



DIP(D6, P5), SOIC (S5), QSOP (Q5)

'FCT2574T **Top View**



LCC(L61)

3

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[5]			0.2		V		All Inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
5. This parameter is guaranteed but not tested.
6. See Figure 11 in AC Loading and Waveforms.
7. One output switching under no load condition.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[8]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[9], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[10]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[12]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[11]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[11]	mA	V_{CC} = MAX, f_0 = 10MHz 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

TRUTH TABLE

Inputs			Outputs 'FCT2374T–'FCT2574T
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH clock transition
Z = HIGH Impedance

Notes:

8. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_1 = Input Frequency
    N_1 = Number of Inputs at f_1
    All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Sym.	Parameter	'FCT2374T-'FCT2574T				'FCT2374AT-'FCT2574AT				'FCT2374CT-'FCT2574CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
t_{PLH} t_{PHL}	Prop. Delay Clock to Output	2.0	11.0	2.0	10.0	2.0	7.2	2.0	6.5	2.0	6.0	2.0	5.2	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time	1.5	14.0	1.5	12.5	1.5	7.5	1.5	6.5	1.5	6.9	1.5	6.2	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	8.0	1.5	8.0	1.5	6.5	1.5	5.5	1.5	6.5	1.5	5.0	ns	1,7,8

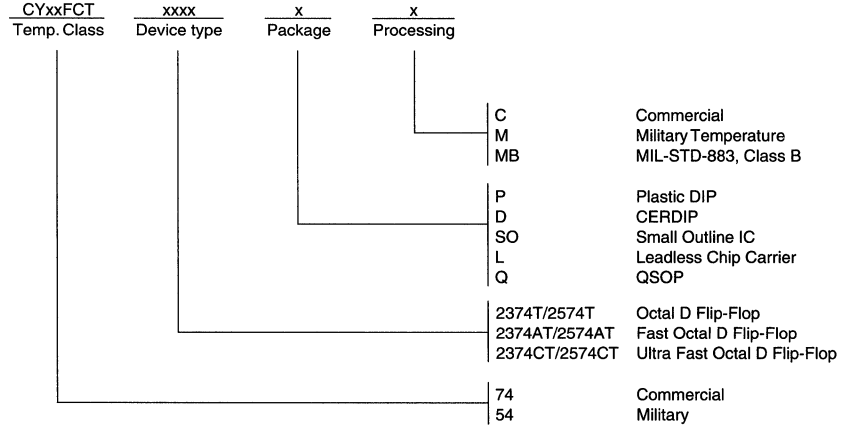
AC CHARACTERISTICS

Sym.	Parameter	'FCT2374T–'FCT2574T				'FCT2374AT–'FCT2574AT				'FCT2374CT–'FCT2574CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.	Min.[13]	Max.		
$t_S(H)$ $t_S(L)$	Setup Time, High or Low D_n to CP	2.0	–	2.0	–	2.0	–	2.0	–	2.0	–	1.5	–	ns	4
$t_n(H)$ $t_n(L)$	Hold Time, High or Low D_n to CP	1.5	–	1.5	–	1.5	–	1.5	–	1.0	–	1.0	–	ns	
$t_W(H)$ $t_W(L)$	Clk Pulse Width[14] High or Low	7.0	–	7.0	–	6.0	–	5.0	–	5.0	–	4.0	–	ns	5

Notes:
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. With one data channel toggling, $t_w(L) = t_w(H) = 4.0$ns and $t_r = t_f = 1.0$ns.

*Refer to the 'Parameter Measurement Information' section of this book. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

ORDERING INFORMATION



CY54/74FCT2541T
8-BITBUFFER/LINE DRIVER

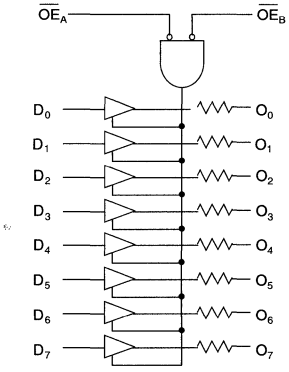
FEATURES

- **Function and pinout compatible with the FCT and F Logic**
- **FCT-C speed at 4.1ns max. (Com'l)**
  FCT-A speed at 4.8ns max. (Com'l)
- **25Ω output series to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l), 12 mA (Mil)**
  15 mA Source Current (Com'l), 12 mA (Mil)
- **3-State Outputs**

DESCRIPTION

The 'FCT2541T is an octal buffer and line driver designed to be employed as a memory address driver, clock driver, and bus-oriented transmitter/receiver. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2541T can be used to replace the 'FCT541T to reduce noise in an existing design. The speed of the 'FCT2541T is comparable to bipolar logic counterparts while reducing power dissipation. The input and output voltage levels allow direct interface with TTL, NMOS, and CMOS devices without external components.

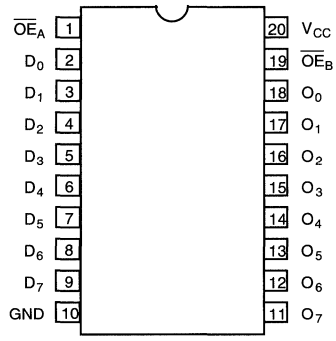
FUNCTIONAL BLOCK DIAGRAM



'FCT2541T

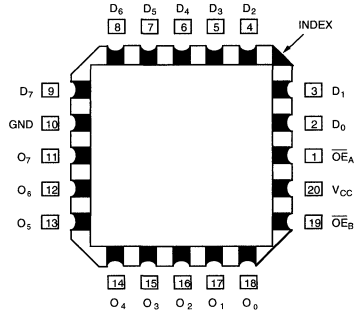
PIN CONFIGURATIONS

TOP VIEW



DIP (D6, P5), SOIC (S5), QSOP (Q5)

TOP VIEW



LCC (L61)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				15	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[8]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_A$ = $\overline{OE}_B$ = GND, or $\overline{OE}_A$ = GND, OE_B = V_{CC} V_{IN} = 3.4V or V_{IN} = GND

TRUTH TABLES

'FCT2541T			
Inputs			Output
$\overline{OE}_A$	OE_B	D	
L	L	L	L
L	L	H	H
H	H	X	Z

H = HIGH Voltage Level,
L = LOW Voltage Level,
X = Don't Care,
Z = High Impedance

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$

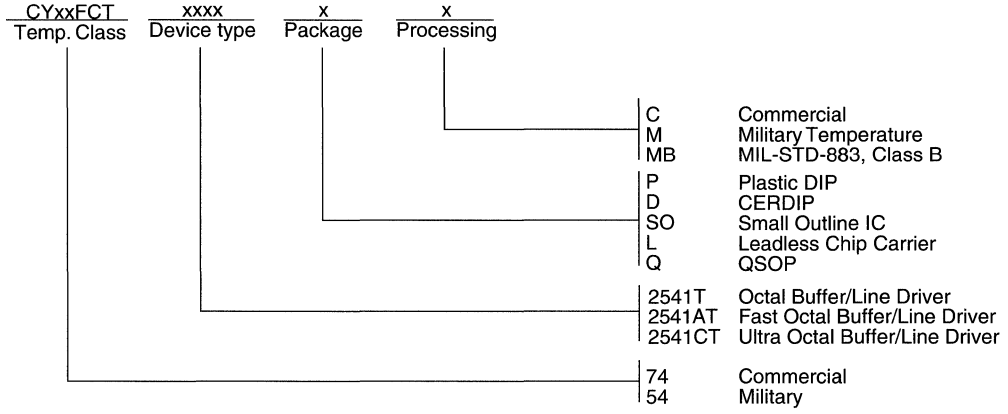
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS (CY54/74FCT2541T)

Symbol	Parameter	'FCT2541T				'FCT2541AT				'FCT2541CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5	9.0	1.5	8.0	1.5	5.1	1.5	4.8	1.5	4.6	1.5	4.1	ns	1, 2
t_{PZH} t_{PZL}	Output Enable Time	1.5	10.5	1.5	10.0	1.5	6.5	1.5	6.2	1.5	6.5	1.5	5.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time	1.5	10.0	1.5	9.5	1.5	5.9	1.5	5.6	1.5	5.7	1.5	5.2	ns	

11. Minimum limits are guaranteed but not tested on propagation delays.
*Refer to the 'Parameter Measurement Information' section of this book. AC characteristics guaranteed with C_L = 50pF.

ORDERING INFORMATION



CY54/74FCT2543T
8-BIT LATCHED TRANSCEIVER

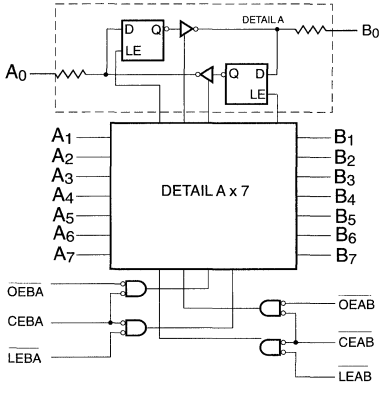
FEATURES

- **Function and Pinout Compatible with the FCT and F Logic**
- **FCT-C speed at 5.3ns max. (Com'l) FCT-A speed at 6.5ns max. (Com'l)**
- **R25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l), 12 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Separate Controls for Data Flow in Each Direction**
- **Back to Back Latches for Storage**

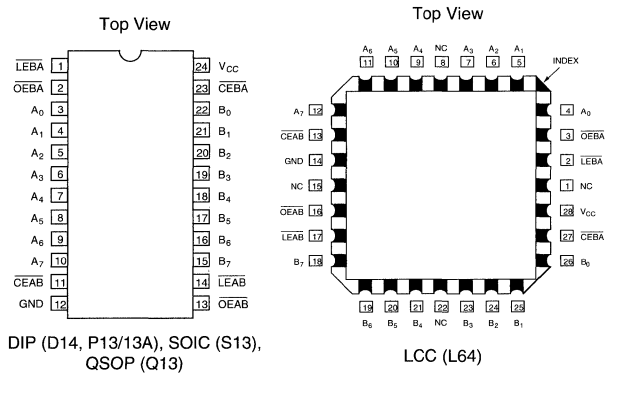
DESCRIPTION

The 'FCT2543T Octal Registered Transceiver contains two sets of eight D-type latches. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) controls permit each latch set to have independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW to enter data from A0–A7 or to take data from B0–B7, as indicated in the truth table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in storage mode and their output no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$ and $\overline{OEAB}$ inputs. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2543T can be used to replace the 'FCT543T to reduce noise in an existing design.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN DESCRIPTIONS

Pin Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

ABSOLUTE MAXIMUM RATINGS[1,2]

Sym	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[5]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_{IH}	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current	Except I/O Pins			5	µA	MAX	V_{IN} = 2.7V
		I/O Pins			15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current	Except I/O Pins			–5	µA	MAX	V_{IN} = 0.5V
		I/O Pins			–15	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				15	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ.[6]	Max.	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[7], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[8]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, $\overline{CEAB}$ + $\overline{OEAB}$ = Low, Outputs Open, $\overline{CEAB}$ = High, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[10]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High One Bit Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[9]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[9]	mA	V_{CC} = MAX, f_0 = 10MHz, $\overline{CEAB}$ + $\overline{OEAB}$ = Low 50% Duty Cycle, Outputs Open, $\overline{CEBA}$ = High Eight Bits Toggling at f_1 = 5MHz, f_0 = $\overline{LEAB}$ = 10MHz, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Typical values are at V_{CC} = 5.0V, +25°C ambient.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE FOR A-TO-B (Symmetric with B-to-A)

Inputs			Latch Status	Outputs 'FCT2543T
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B0–B7
H	–	–	Storing	High Z
–	H	–	Storing	–
–	–	H	–	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs

* = Before $\overline{LEAB}$ LOW-to-HIGH Transition
H = HIGH Voltage Level
L = LOW Voltage Level
– = Don't Care or Irrelevant
A-to-B data flow shown: B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$

AC CHARACTERISTICS

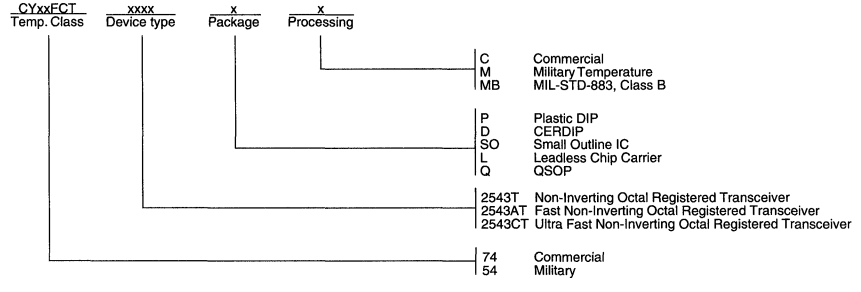
Sym.	Parameter	'FCT2543T				'FCT2543AT				'FCT2543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	2.0	10.0	2.5	8.5	2.5	7.5	2.5	6.5	2.5	6.1	2.5	5.5	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A_n $\overline{LEAB}$ to B_n	2.5	14.0	2.5	12.5	2.5	9.0	2.5	8.0	2.5	8.0	2.5	7.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	14.0	2.0	12.0	2.0	10.0	2.0	9.0	2.0	9.0	2.0	8.0	ns	1,7,8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	2.0	13.0	2.0	9.0	2.0	8.5	2.0	7.5	2.0	7.5	2.0	6.5	ns	1,7,8

AC OPERATING REQUIREMENTS

Sym.	Parameter	'FCT2543T				'FCT2543AT				'FCT2543CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.	Min.[11]	Max.		
t_s (H) t_s (L)	Set-up Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	3.0	—	3.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	9
t_w	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	6

Note:
11. Minimum limits are guaranteed on Propagation Delays.
*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION



CY54/74FCT2646T
CY54/74FCT2648T
8-BIT REGISTERED TRANCEIVERS

FEATURES

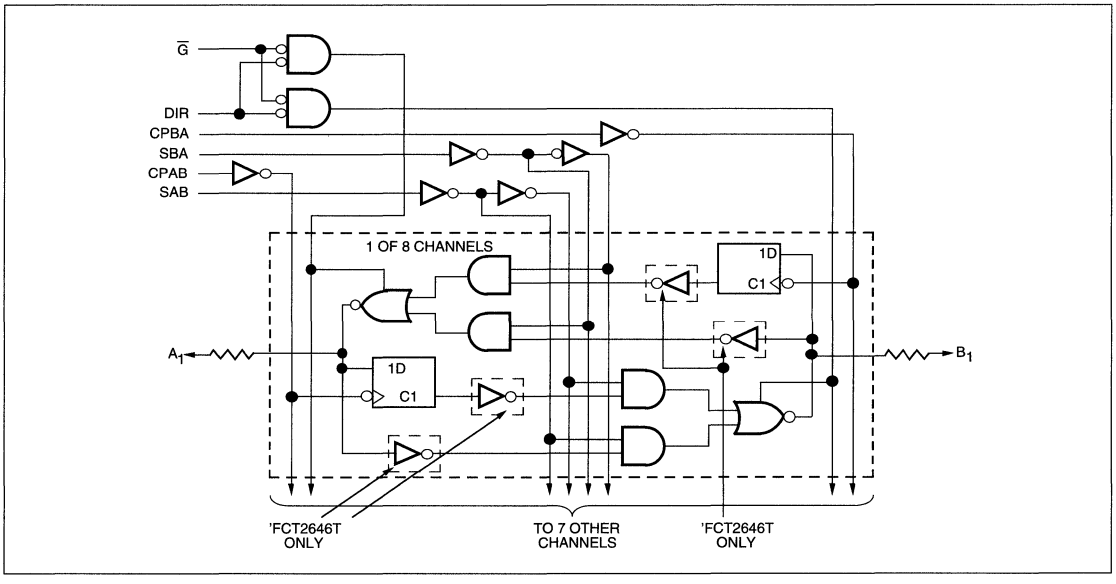
- **Function and Pinout Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Commercial) FCT-A speed at 6.3ns max. (Commercial)**
- **R25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l and Mil) 15 mA Source Current (Com'l and Mil)**
- **Independent Register for A and B Buses**
- **3-State Output**

DESCRIPTION

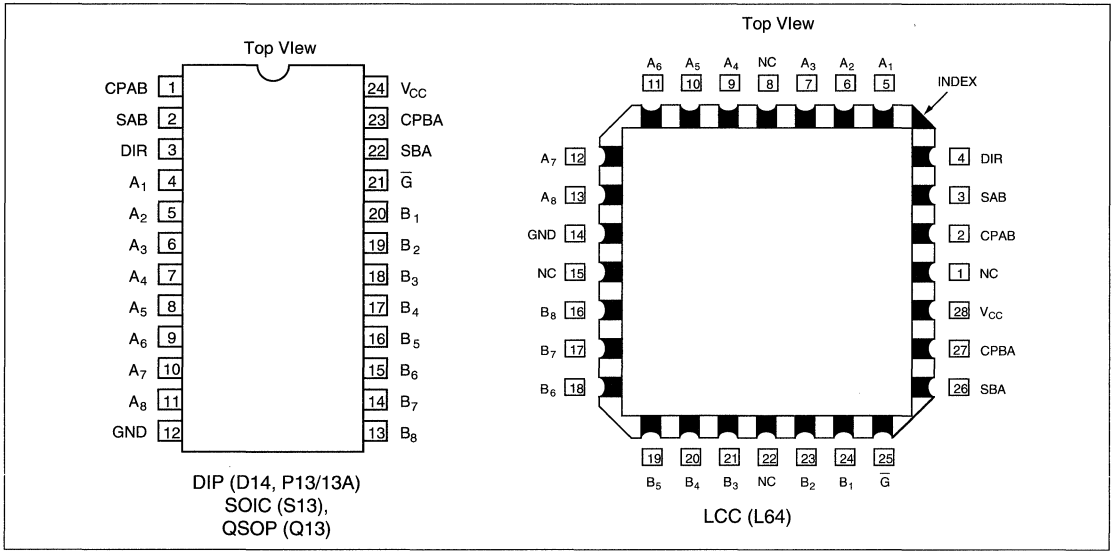
The 'FCT2646T and 'FCT2648T consist of a bus tranceiver circuit with 3-state, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a high logic level. Enable Control $\overline{G}$ and direction pins are provided to control the transceiver function. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections so that the 'FCT2646T and the 'FCT2648 can be used to replace the 'FCT646T and the 'FCT648, respectively, in an existing design.

In transceiver mode, data present at the high impedance port may be stored in either A or B register, or in both. Select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus receives data when enable control $\overline{G}$ is Active LOW. In isolation mode (enable Control $\overline{G}$ HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

FUNCTIONAL BLOCK DIAGRAM



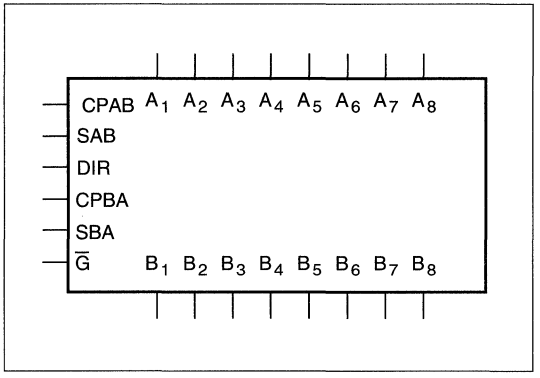
PIN CONFIGURATIONS

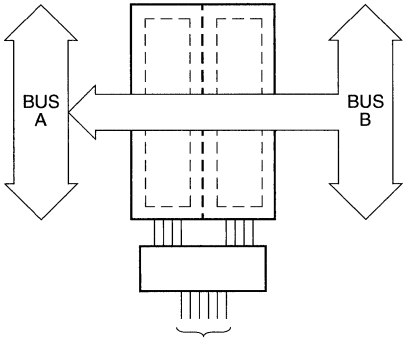


PIN DESCRIPTION

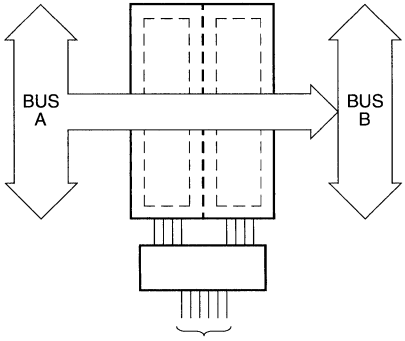
Pin Names	Description
A_1 - A_8	Data Register A Inputs Data Register B Outputs
B_1 - B_8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs

LOGIC SYMBOL

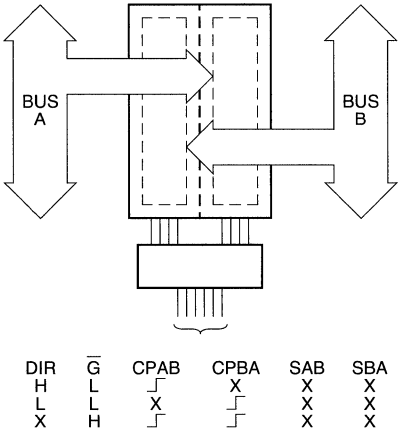




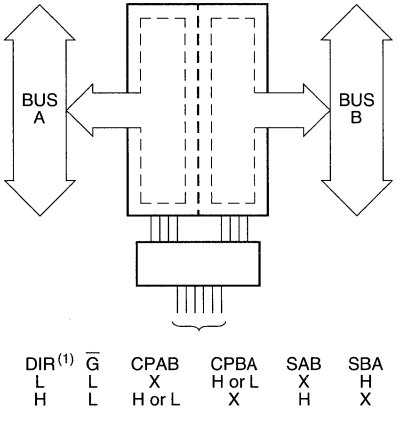
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

Note: Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLE

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'$FCT2646T	'$FCT2648T
H H	X X	H or L ↓	H or L ↓	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time B Data to A Bus Stored B Data to A Bus	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real Time A Data to B Bus Stored A Data to B Bus	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus

Notes:
1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.
2. H = HIGH, L = LOW, X = Don't Care, ↓ = LOW-to-HIGH Transition

ABSOLUTE MAXIMUM RATINGS[3,4]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[5]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[6]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[7]			6	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[7]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

3. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typicalvalues are at V_{CC} = 5.0V, T_A = +25°C ambient.
6. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
7. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[8], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[9]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[11]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, $\overline{G}$ = DIR = GND, or GAB = $\overline{GBA}$ = GND, V_{IN} = 3.4V or V_{IN} = GND

Notes:

8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_1 = Input Frequency
    N_1 = Number of Inputs at f_1
    All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT2646T/2648T				'FCT2646AT/2648AT				'FCT2646CT/2648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay[13] Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 3
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus and DIR to A or B	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{G}$ to Bus and DIR to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 5

AC OPERATING REQUIREMENTS

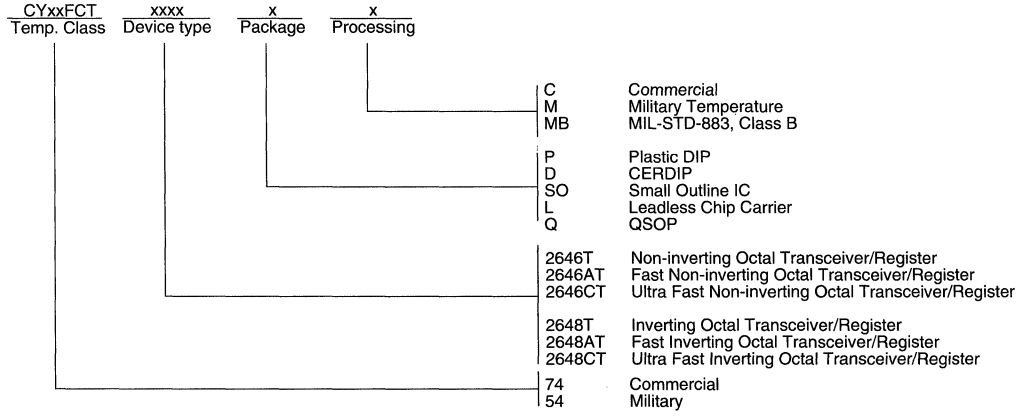
Symbol	Parameter	'FCT2646T/2648T				'FCT2646AT/2648AT				'FCT2646CT/2648CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	4
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	5

Note:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION



CY54/74FCT2652T
8-BIT REGISTERED TRANSCEIVER

FEATURES

- **Function and Drive Compatible with the FCT and F Logic**
- **FCT-C speed at 5.4ns max. (Com'l) FCT-A speed at 6.3ns max. (Com'l)**
- **R25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l), 12 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Independent Register for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfer**
- **Bidirectional Bus Transceiver and Registers**

DESCRIPTION

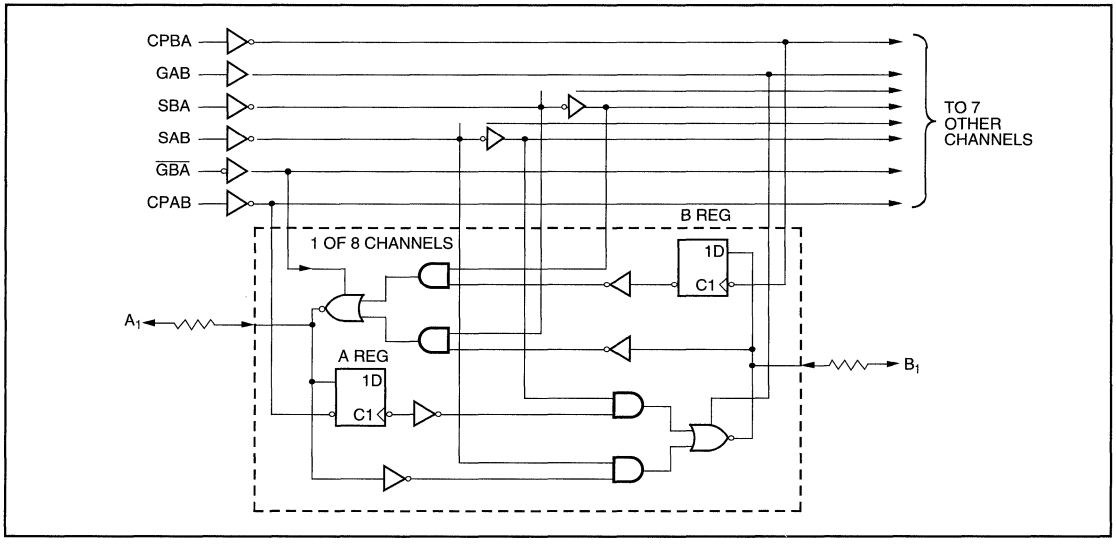
The 'FCT2652T consists of bus tranciever circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. GAB and $\overline{GBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

On-chip termination resistors are added to the outputs to reduce system noise caused by reflections. The 'FCT2652T can replace the 'FCT652T to reduce noise in an existing design.

The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during transition between stored and real-time data. A low input level selects real-time data and a high selects stored data.

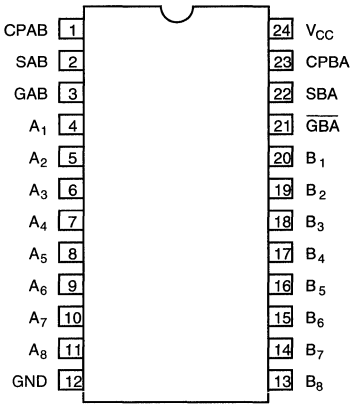
Data on the A or B data bus, or both, can be stored in internal D flip-flops by low-to-high transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins. By simultaneously enabling GAB and $\overline{GBA}$ when SAB and SBA are in real-time transfer mode, it is possible to store data without using internal D-type flip-flops. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last state.

FUNCTIONAL BLOCK DIAGRAM



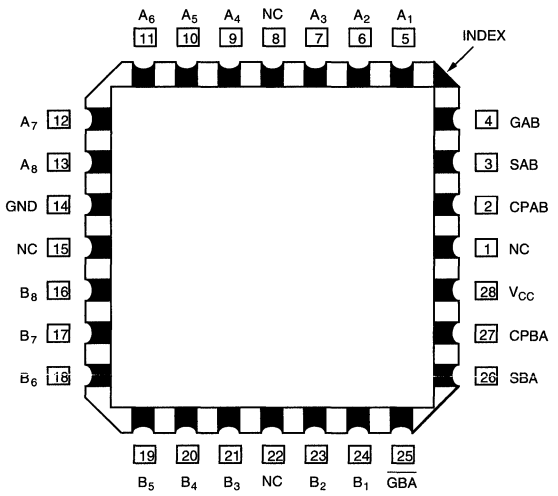
PIN CONFIGURATIONS

Top View



DIP (D14, P13/13A) SOIC (S13), QSOP(Q13)

Top View



LCC (L64)

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

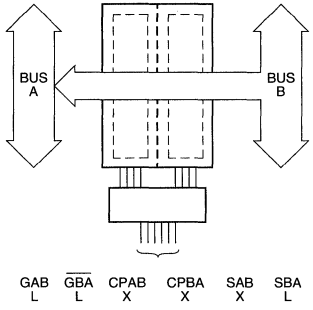
Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

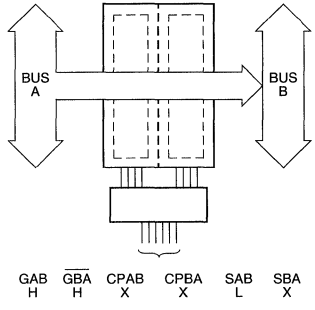
Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.55	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.55	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[5]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

Notes:

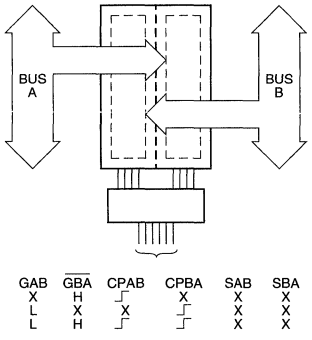
1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.



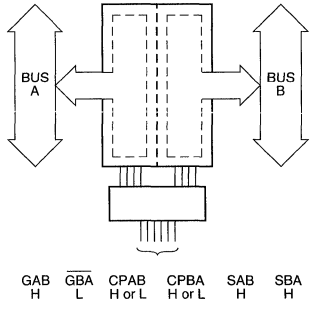
REAL-TIME TRANSFER BUS B TO BUS A



REAL-TIME TRANSFER BUS A TO BUS B



STORAGE FROM A AND/OR B



TRANSFER STORED DATA TO A AND/OR B

Note: Cannot transfer data to A bus and B bus simultaneously.

FUNCTION TABLES

Inputs						Data I/O		Operation or Function
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 thru A_8	B_1 thru B_8	'FCT2652T
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↓	↓	X	X			Store A and B Data
X	H	↓	H or L	X	X	Input	Unspecified[6]	Store A, Hold B
H	H	↓	↓	X[7]	X	Input	Output	Store A in both registers
L	X	H or L	↓	X	X	Unspecified[1]	Input	Hold A, Store B
L	L	↓	↓	X	X[7]	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:

6. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
7. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.

H = HIGH, L = LOW, X = Don't Care, ↓ LOW-to-HIGH Transition

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[8], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[9]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open GAB = GND, $\overline{GBA}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[11]	1.7	4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.2	6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, GAB = GND, $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		7.0	12.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 0.2V or $V_{IN} \geq V_{CC} - 0.2V$
		9.2	21.8[10]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 5MHz, GAB = $\overline{GBA}$ = GND, SAB = CPAB = GND, SBA = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

Notes:

8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} \bullet D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_1 = Input Frequency
    N_1 = Number of Inputs at f_1
    All currents are in milliamps and all frequencies are in megahertz.

AC CHARACTERISTICS

Symbol	Parameter	'FCT2652T				'FCT2652AT				'FCT2652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	6.0	1.5	5.4	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time Enable to Bus	2.0	15.0	2.0	14.0	2.0	10.5	2.0	9.8	1.5	8.9	1.5	7.8	ns	1, 5
t_{PHZ} t_{PLZ}	Output Disable Time Enable to Bus	2.0	11.0	2.0	9.0	2.0	7.7	2.0	6.3	1.5	7.7	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	2.0	10.0	2.0	9.0	2.0	7.0	2.0	6.3	1.5	6.3	1.5	5.7	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to A or B	2.0	12.0	2.0	11.0	2.0	8.4	2.0	7.7	1.5	7.0	1.5	6.2	ns	1, 7, 8

Notes:

* AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

* See "Parameter Measurement Information" in the General Information Section.

AC OPERATING REQUIREMENTS

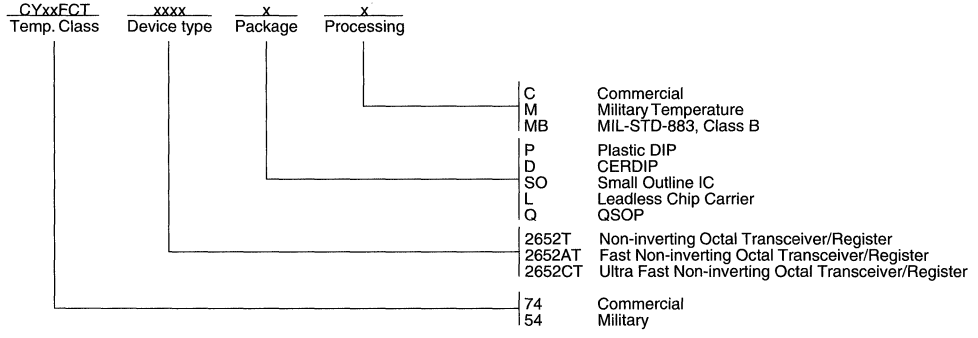
Symbol	Parameter	'FCT2652T				'FCT2652AT				'FCT2652CT				Units	Fig. No.*
		MIL		COM'L		MIL		COM'L		MIL		COM'L			
		Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.	Min.[12]	Max.		
$t_s(H)$ $t_s(L)$	Setup Time HIGH or LOW Bus to Clock	4.5	—	4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns	1, 4
$t_h(H)$ $t_h(L)$	Hold Time HIGH or LOW Bus to Clock	2.0	—	2.0	—	1.5	—	1.5	—	1.5	—	1.5	—	ns	1, 4
$t_w(H)$ $t_w(L)$	Clock Pulse Width, HIGH or LOW	6.0	—	6.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns	1, 5

Notes:

12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. With one data channel toggling, $t_w(L) = t_w(H)$ = 4.0ns and $t_r = t_f$ = 1.0ns.

*Refer to the 'Parameter Measurement Information' section of this book.

ORDERING INFORMATION



CY54/74FCT2827T
10-BIT BUFFER

FEATURES

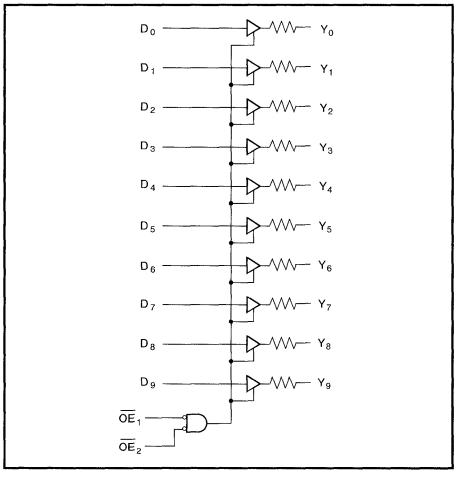
- **Function and Drive Compatible with the FCT, F and AM29827 Logic**
- **FCT-B speed at 5.0ns max. (Commercial) FCT-A speed at 8.0ns max. (Commercial)**
- **R25Ω output series resistors to reduce transmission line reflection noise**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **12 mA Sink Current (Com'l), 12 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**

DESCRIPTION

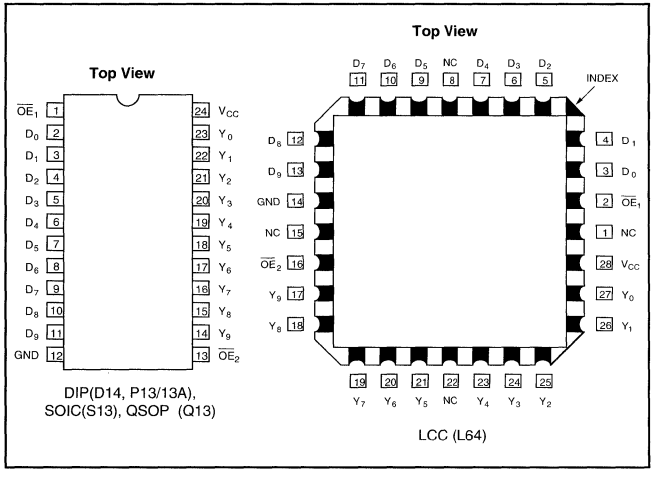
The 'FCT2827T 10-bit bus driver provides high-performance bus interface buffering for wide data/address paths or buses carrying parity. This 10-bit buffer has NOR-ed output enables for maximum control flexibility. The non-inverting 'FCT2827T is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high-impedance state. On-chip termination resistors have been added to the outputs to reduce system noise caused by reflections. The 'FCT2827T can be used to replace the 'FCT827T to reduce noise in an existing design.

3

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[3]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 12mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 12mA
R_{OUT}	Output Resistance	Military		25		Ω	MIN	I_{OL} = 12mA
		Commercial	20	25	40	Ω	MIN	I_{OL} = 12mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[4]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[5]			6	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[5]			8	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}$–0.2V

Notes:

1. Operation beyond the values set forth in the above table may impair the useful life of the device. Unless otherwise noted, these values are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
3. Typical values are at V_{CC} = 5.0V, T_A = +25°C ambient.
4. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
5. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[3]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[6], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[7]	0.15	0.25	mA/ MHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
I_C	Total Power Supply Current[9]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ – 0.2V
		5.2	14.5[8]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}_1$ = $\overline{OE}_2$ = GND, V_{IN} = 3.4V or V_{IN} = GND

Notes:

6. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
8. Values for these conditions are examples of the I_{CC} formula. These values are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1

All currents are in milliamps and all frequencies are in megahertz.

FUNCTION TABLES

'FCT2827T (Non-Inverting)

Inputs			Outputs	Function
$\overline{OE}_1$	$\overline{OE}_2$	D_i	Y_i	
L	L	L	L	Transparent
L	L	H	H	
H	X	X	Z	Three-State
X	H	X	Z	

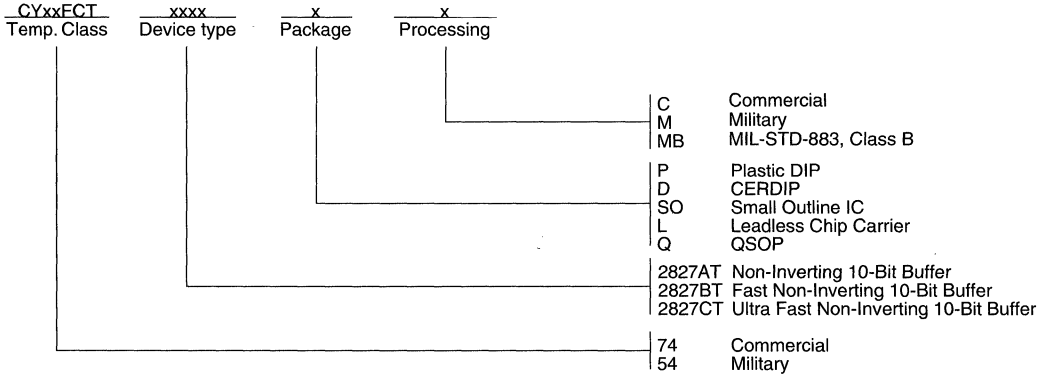
Note:
H = High, L = Low, X = Don't Care, Z = High Impedance

AC CHARACTERISTICS

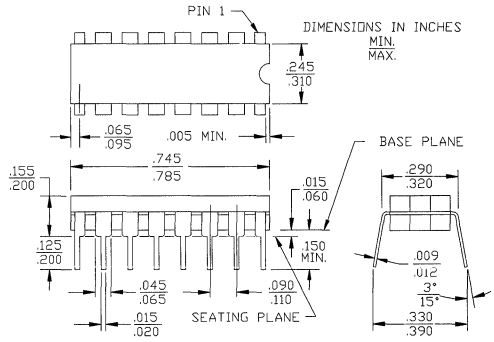
Sym.	Parameter	Test Conditions	'FCT2827AT				'FCT2827BT				Units	Fig. No.*
			MIL		COM'L		MIL		COM'L			
			Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.	Min.[10]	Max.		
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1	C_L = 50pF R_L = 500Ω	–	9.0	–	8.0	–	6.5	–	5.0	ns	1,3
t_{PLH} t_{PHL}	Propagation Delay from D_1 to Y_1	C_L = 300pF[11] R_L = 500Ω	–	17.0	–	15.0	–	14.0	–	13.0	ns	1,3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 50pF R_L = 500Ω	–	13.0	–	12.0	–	9.0	–	8.0	ns	1,2
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_1	C_L = 300pF[11] R_L = 500Ω	–	25.0	–	23.0	–	16.0	–	15.0	ns	1,2
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 5pF[11] R_L = 500Ω	–	10.0	–	9.0	–	7.0	–	6.0	ns	1,7,8
t_{PHZ} t_{PHL}	Output Disable Time $\overline{OE}$ to Y_1	C_L = 50pF[11] R_L = 500Ω	–	10.0	–	9.0	–	8.0	–	7.0	ns	1,7,8

Notes:
10. Minimum values are guaranteed but not tested on Propagation Delays.
11. These parameters are guaranteed but not tested.
*Refer to the 'Parameter Measurement Information' section of this book.

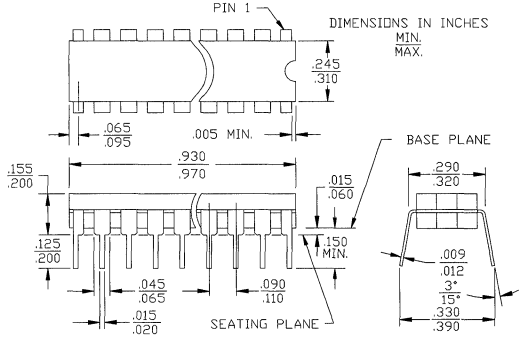
ORDERING INFORMATION



16-Lead (300-Mil) CerDIP D2
MIL–STD–1835 D–2 Config. A



20-Lead (300-Mil) CerDIP D6
MIL–STD–1835 D–8 Config. A



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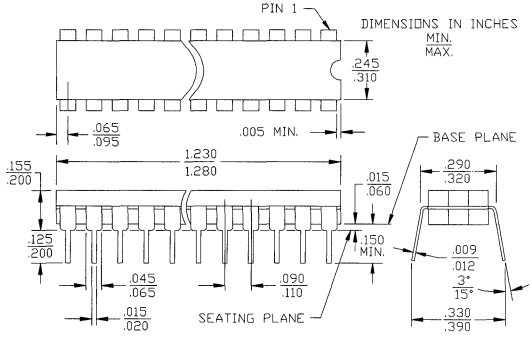
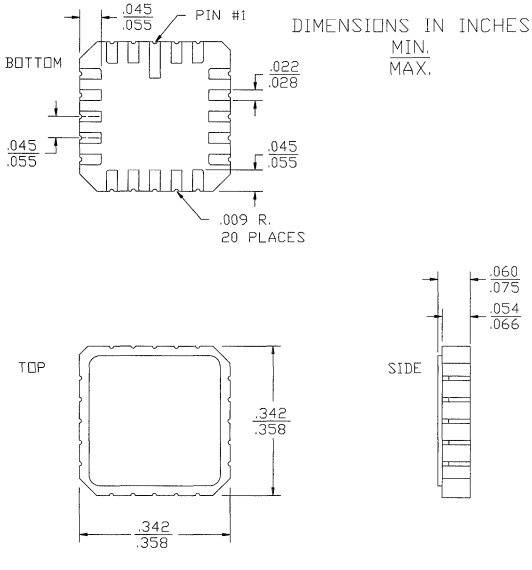
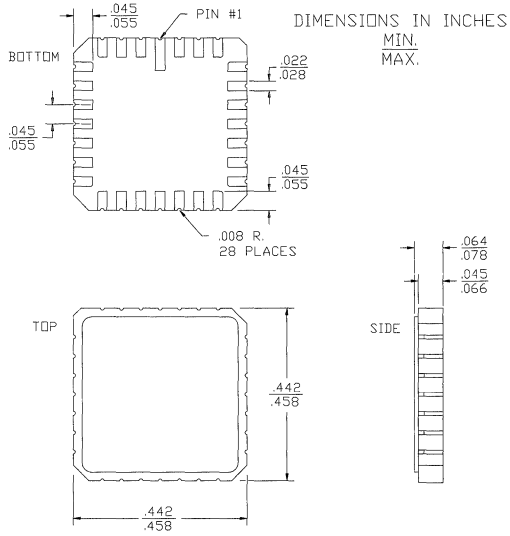
MIL–STD–1835 D–9 Config. A



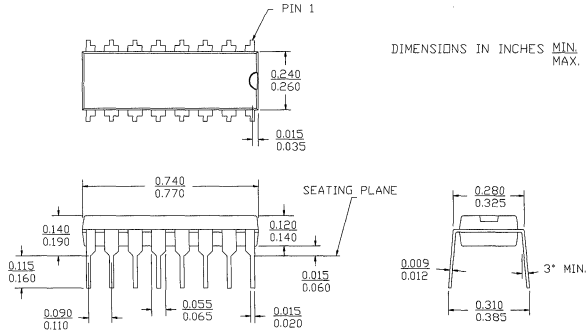
20-Pin Square Leadless Chip Carrier L61
MIL–STD–1835 C–2A



28-Square Leadless Chip Carrier L64
MIL–STD–1835 C–4



16-Lead (300-Mil) Molded DIP P1



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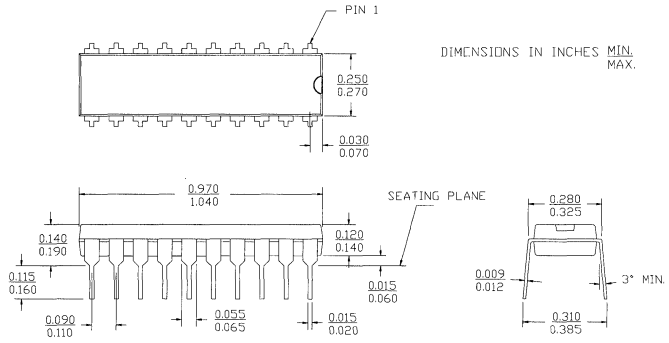
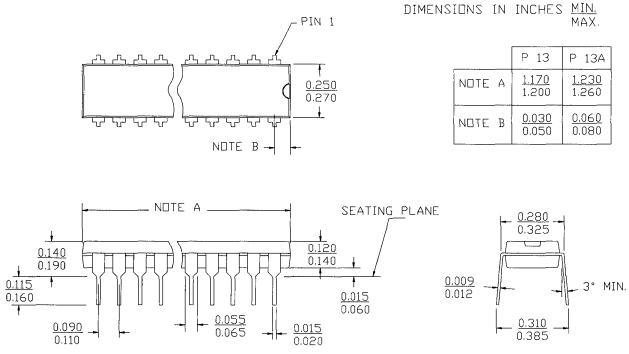
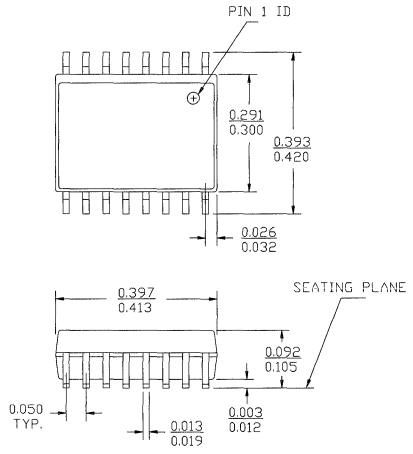


24-Lead (300-Mil) Molded DIP P13/P13A



	P 13	P 13A
NOTE A	1.170 1.200	1.230 1.260
NOTE B	0.030 0.050	0.060 0.080

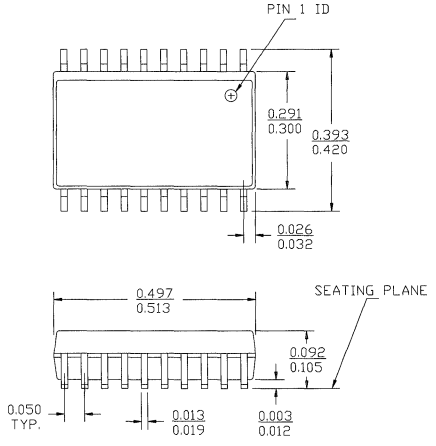
16-Lead Molded SOIC S1



DIMENSIONS IN INCHES MIN.
MAX.

LEAD COPLANARITY 0.004 MAX.

20-Lead (300-Mil) Molded SOIC S5



DIMENSIONS IN INCHES MIN.
MAX.

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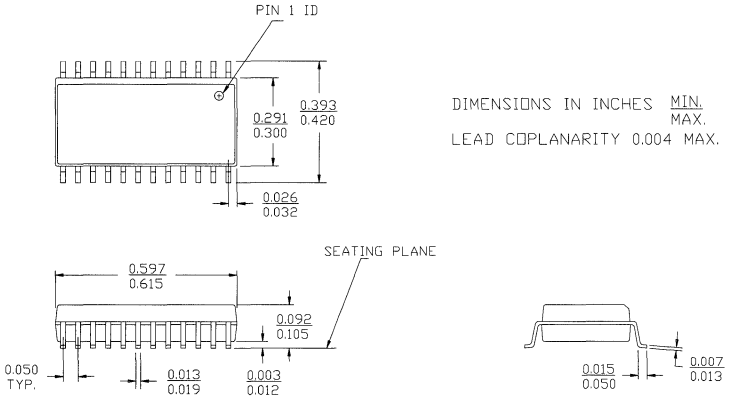
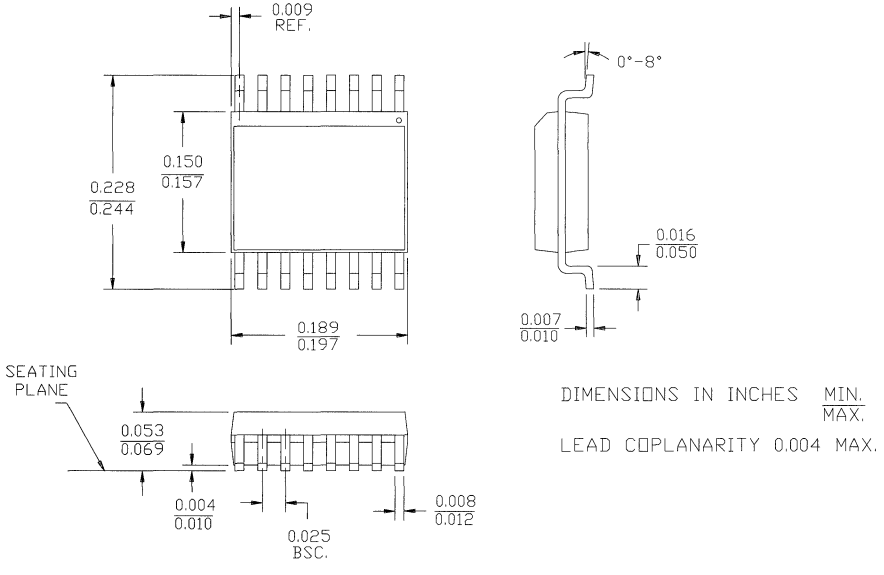
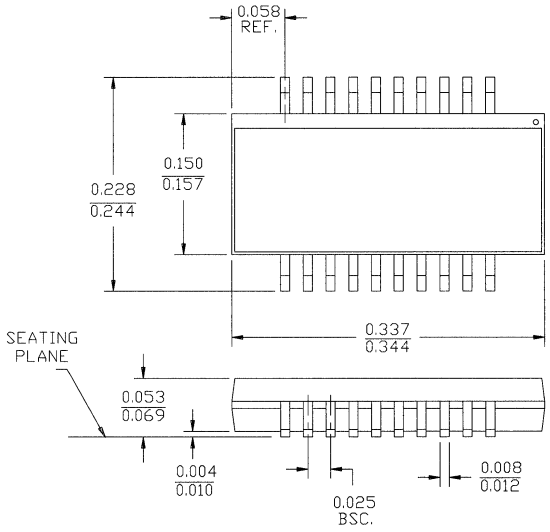
24-Lead (300-Mil) Molded SOIC S13

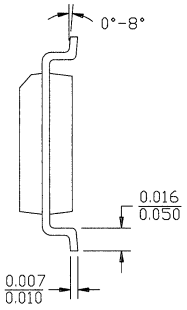


16-Lead Quarter Size Outline Q1



20-Lead Quarter Size Outline Q5

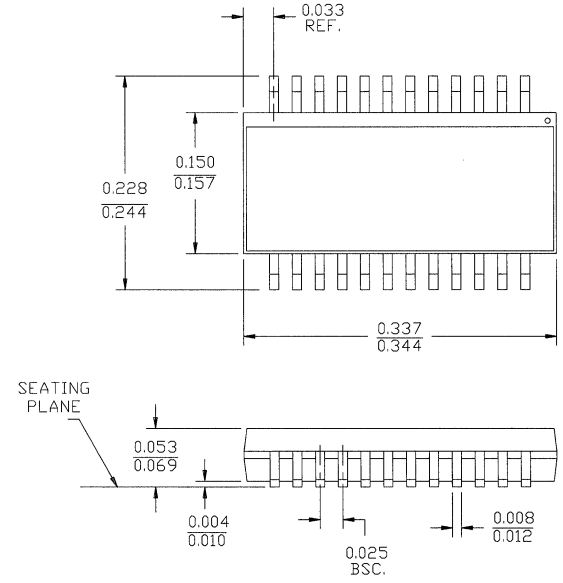


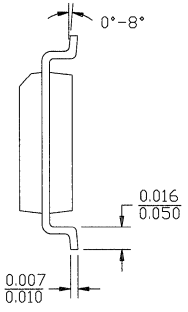


DIMENSIONS IN INCHES MIN./MAX.

LEAD COPLANARITY 0.004 MAX.

24-Lead Quarter Size Outline Q13





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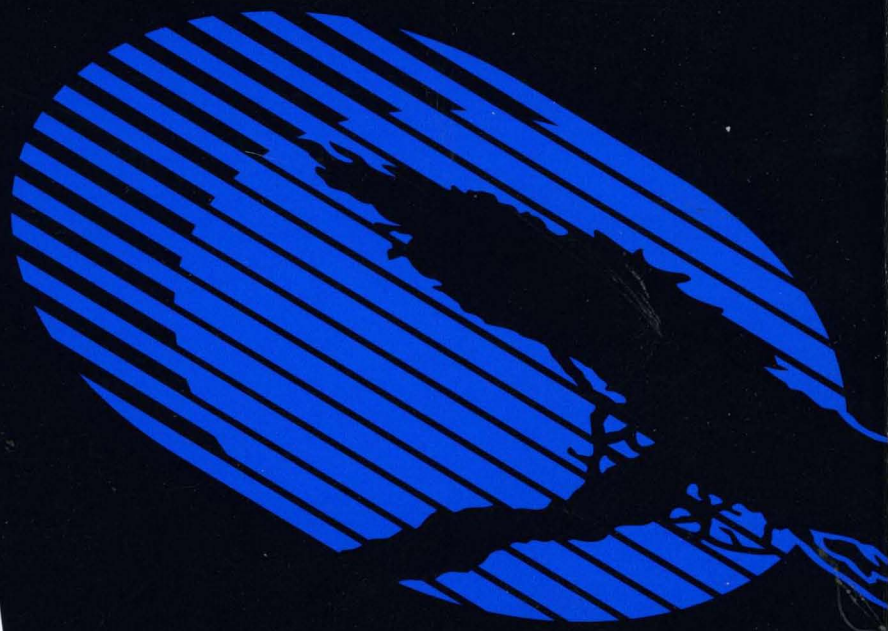

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